

LV550 AMD Schematics

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference



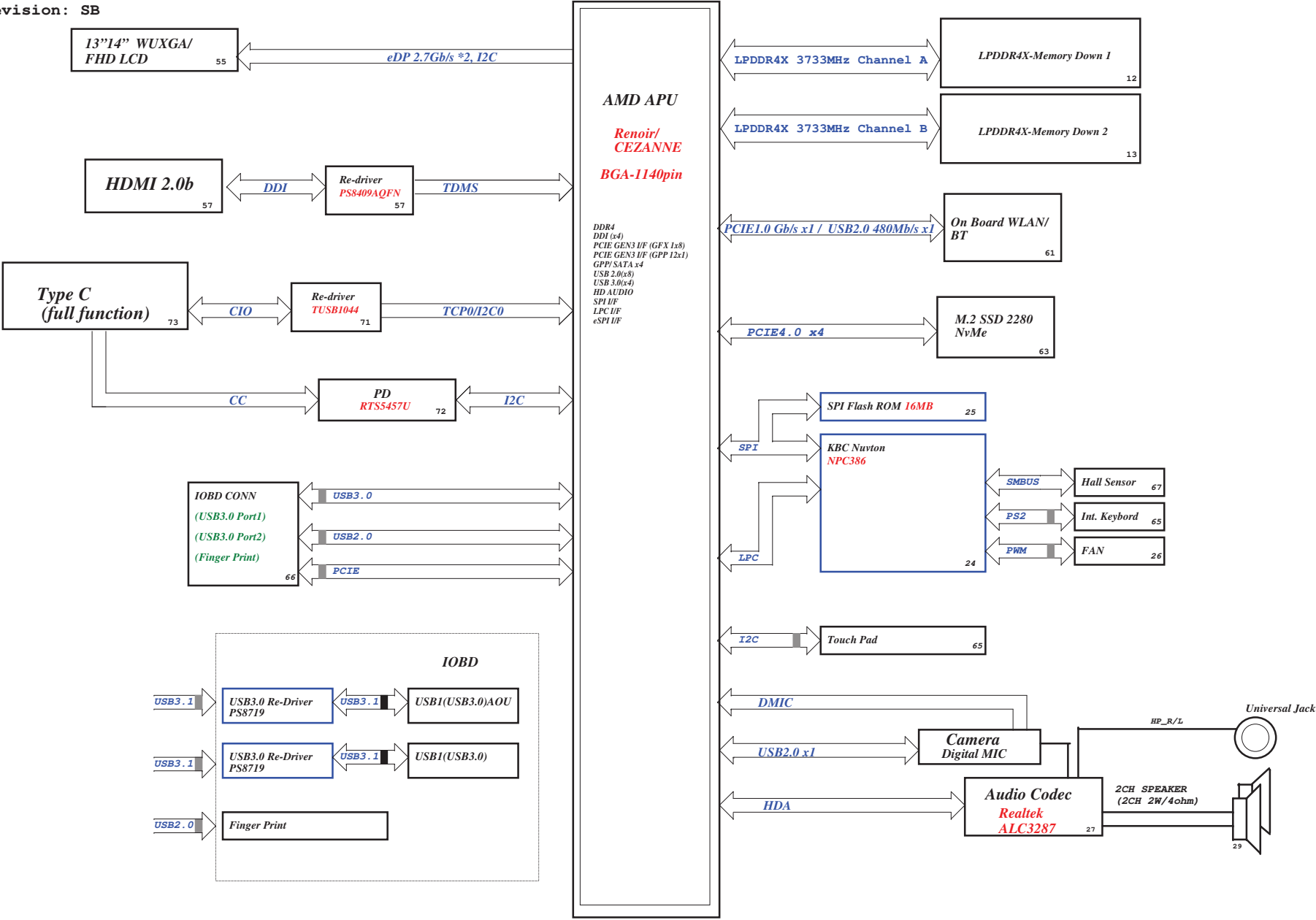
BOM control name
Part reference
Symbol name

Properties

DY	DUMMY, NOT ASM, not assemble
MEM_IDx_x	Memory ID for SW Team (BOM Control)
PCB_ID	PCB ID for SW Team (PCB version)
SKU_ID	SKU ID for SW Team (Model ID)
HDT	Debug Connector
PSL	KBC Power Switched Logic
MS/ NON_MS	Modern stand by / NON Modern stand by
TPM	TPM

AMD Cezanne new project code:
LV550-13AC: 4PD0NK010001
LV550-14AC: 4PD0NK01A001
PCB P/N: 203075 13"
203081 14"
Revision: SB

LV550 AMD Block Diagram



PCB Layer Stackup	
L1: Signal	
L2: GND/POWER	
L3: Signal	
L4: Signal	
L5: GND/POWER	
L6: Signal	
L7: GND/POWER	
L8: Signal	
Battery Charger/Selector BQ25710RSNR 44	
PWR_ADP_TOSYS	19V_DCBATOUT RT+
System DC/DC TPS51395PRJER 45	
19V_DCBATOUT	5V_S5 5V_AUX_S5
System DC/DC TPS51393PRJER 45	
19V_DCBATOUT	3D3V_S5 3D3V_AUX_S5
CPU_VCORE RT3664BEGQW 46	
DC/DC VCCPCUCORE AOZ516QI 47	
19V_DCBATOUT	1V_CPU_CORE
DC/DC VCCPCUCORE RT9610BZQW 48	
19V_DCBATOUT	1V_VDDCR_SOC
DC/DC 1D2V_S3 RT8231AGQW 51	
19V_DCBATOUT	1D1V_S3
DC/DC 0D6V_VREF_S0 RT8231AGQW 51	
1D1V_S3	0D6V_S3
DC/DC 0D75V_S5 RT5797ALGQW 52	
3D3V_S5	0D75V_S5
DC/DC 0D75V_S0 RT5797ALGQW 52	
3D3V_S5	0D75V_S0
1D8V_S5 SY8386RHC 53	
19V_DCBATOUT	1D8V_S5

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Title	
CPU (PCIE/SATA)	
Size A3	Document Number Rev SB
Date: Tuesday, April 20, 2011	
Sheet 3 of 106	

D

C

B

A

(Blanking)

LV550AC

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Title		
CPU (RSVD)		
Size	Document Number	Rev
A4	LV550 AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 4 of 106

SSID = CPU

Pinout Details:

- Section D (Pins 1-31):**
 - 12 M_A_DQ[31:0] <<>> (16 pins)
 - 12 M_B_DQ[31:0] <<>> (16 pins)
- Section C (Pins 32-63):**
 - 12 M_A_DQS_DN[3:0] <<>> (4 pins)
 - 12 M_B_DQS_DN[3:0] <<>> (4 pins)
 - 12 M_A_DQS_DP[3:0] <<>> (4 pins)
 - 12 M_B_DQS_DP[3:0] <<>> (4 pins)
- Section B (Pins 64-95):**
 - 12 M_A_CKE0 >>>> (4 pins)
 - 12 M_B_CKE0 >>>> (4 pins)
 - 12 M_A_CKE1 >>>> (4 pins)
 - 12 M_B_CKE1 >>>> (4 pins)
 - 12 M_A_CS0_N >>>> (4 pins)
 - 12 M_B_CS0_N >>>> (4 pins)
 - 12 M_A_CS1_N >>>> (4 pins)
 - 12 M_B_CS1_N >>>> (4 pins)
 - 12 M_A_A0 >>>> (4 pins)
 - 12 M_B_A0 >>>> (4 pins)
 - 12 M_A_A1 >>>> (4 pins)
 - 12 M_B_A1 >>>> (4 pins)
 - 12 M_A_A2 >>>> (4 pins)
 - 12 M_B_A2 >>>> (4 pins)
 - 12 M_A_A3 >>>> (4 pins)
 - 12 M_B_A3 >>>> (4 pins)
 - 12 M_A_A4 >>>> (4 pins)
 - 12 M_B_A4 >>>> (4 pins)
 - 12 M_A_A5 >>>> (4 pins)
 - 12 M_B_A5 >>>> (4 pins)
- Section A (Pins 96-100):**
 - 12 M_A_CLK_P <<<< (4 pins)
 - 12 M_B_CLK_P <<<< (4 pins)
 - 12 M_A_CLK_N <<<< (4 pins)
 - 12 M_B_CLK_N <<<< (4 pins)
 - 12 M_A_DM1 <<<< (4 pins)
 - 12 M_B_DM1 <<<< (4 pins)
 - 12 M_A_DM0 <<<< (4 pins)
 - 12 M_B_DM0 <<<< (4 pins)
 - 12 M_A_RESET_N <<<< (4 pins)

APU Type 2 does not support Channel A

**ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40-60Ω
DDR CLK, 72Ω
DQS, 80Ω**

ADD and CLK on the sam layer

DM, DQ & DQS

DM, DQ & DQS on the same layer

TP501

101V_S3

REN0IR-FP6-GP

**FP6 REV 0.92
PART 1 OF 13**

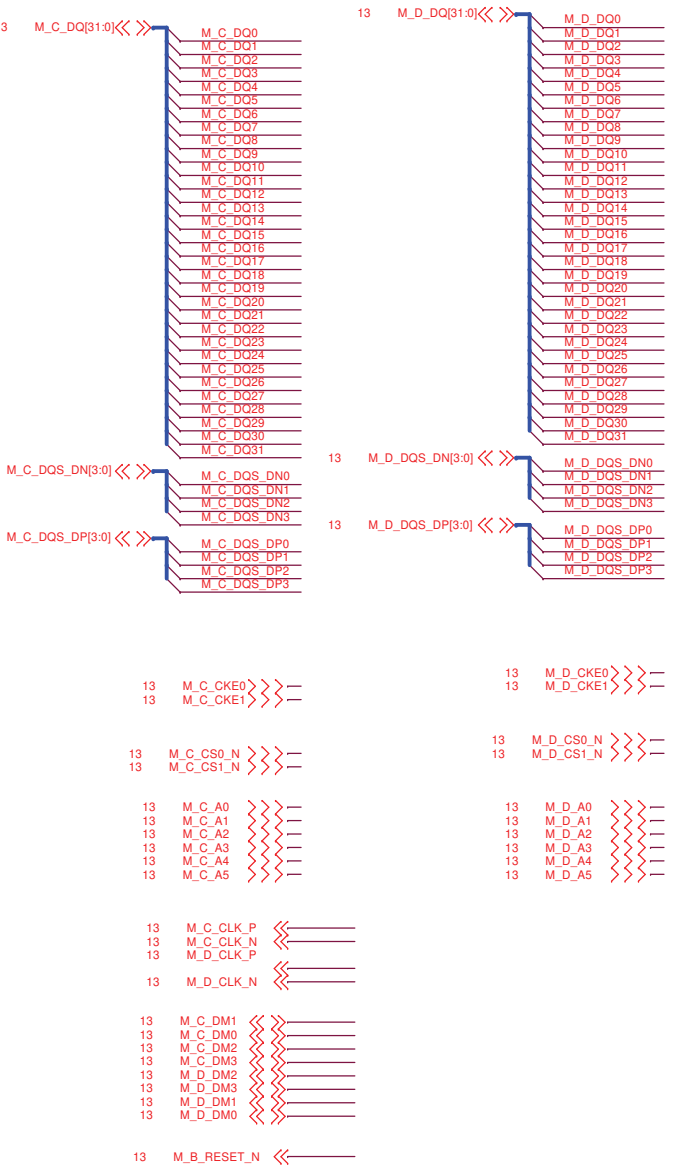
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Follow CRB 20200313

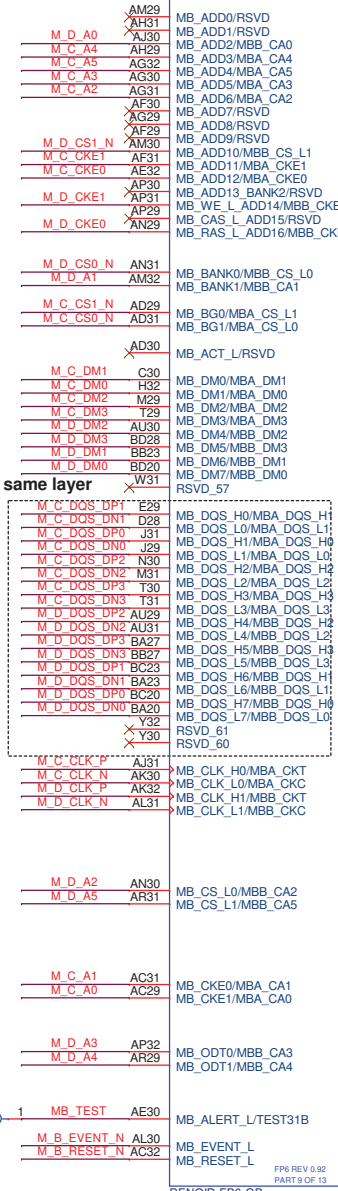
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<p>Title: CPU (DDR4 CHA)</p>		
Size A3	Document Number LV550 AMD	Rev SB
<p>Date: Tuesday, April 20, 2021 Sheet 5 of 106</p>		

Title			
CPU (DDR4 CHA)			
Size A3	Document Number		Rev
	LV550 AMD		SB
Date:	Tuesday, April 20, 2021	Sheet 5 of	106

SSID = CPU



ADD and CLK on the sam layer

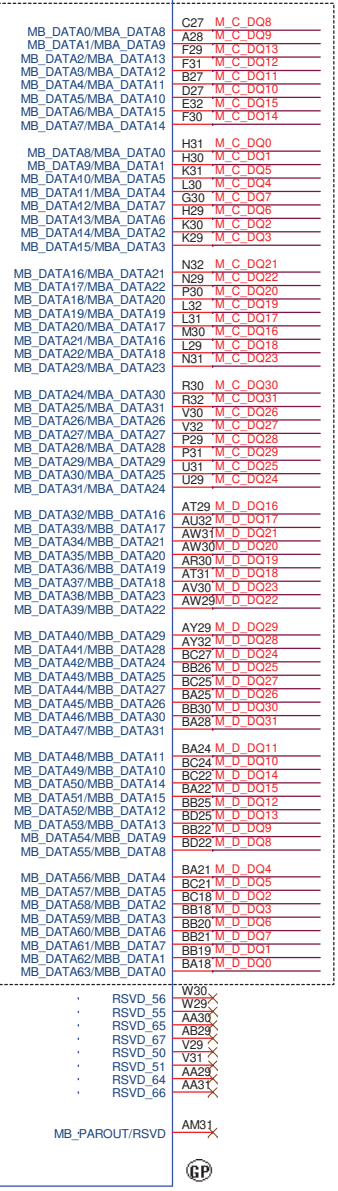


ADD, CMD, CTL, 40Ω
DATA CHECK, 50Ω
Misc. 40~60Ω
DDR CLK, 72Ω
DQS, 80Ω

CPU11

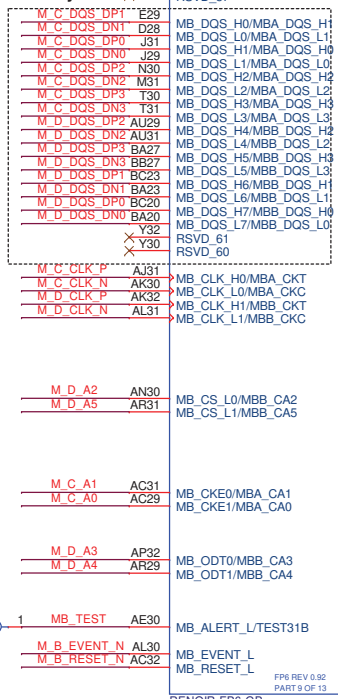
MEMORY 8

DM, DQ & DQS on the same layer



Signal GRP	Signal			
Clocks	CLK			
Address	ADD	BANK	BG	
Command	RAS_L	CAS_L	WE_L	ACT
Control	CKE	ODT	CS_L	
Data	Data	DM	DQS	
Misc.	M_RESET_L M_EVENT_L M_ALERT			
M_PAROUT				

DM, DQ & DQS on the same layer



TP601

1D1V_S3

R601 1

1K2J1-GP

ZZ.00CPU.421

FP6 REV 0.02
PART 9 OF 13



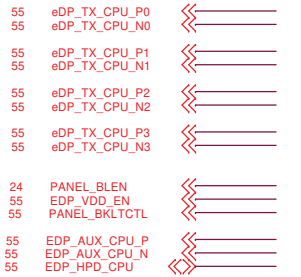
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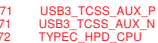
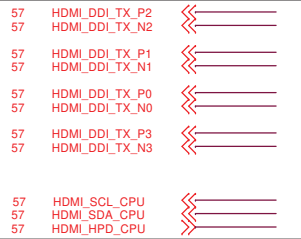
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Size A3	Document Number	LV550 AMD		Rev SB
Date:	Tuesday, April 20, 2021	Sheet	6	of 106

SSID = PCH

eDP



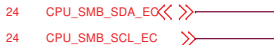
HDMI



HDT

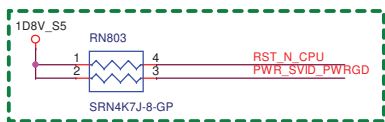


SVID

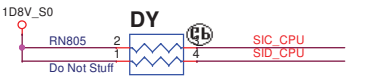
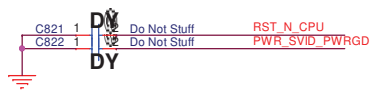
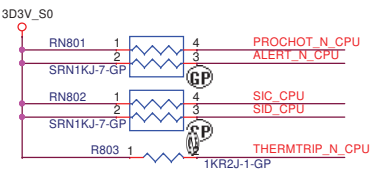
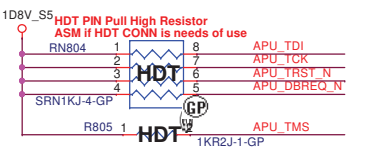


DISPLAY/SVI/JTAG/TEST

APU Type I(CZ): 1D8V
APU Type II(CZ-L): 3D3V



HDT EVT stage要上



RN801 change to 4 pin from 8 pin & add RN802
Add RN803 R5VD SIC/ SID 1D8V_S0 signal
Reserve 1.8v pull up at SIC & SID of CPU (Right now pull up 3.3v)_1

Check list: PD/CRB:PH

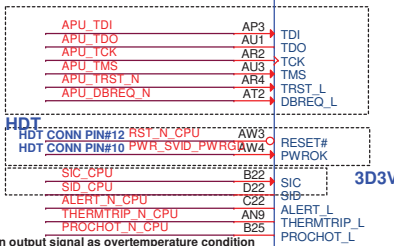


eDP

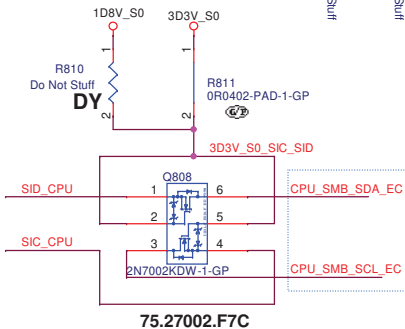
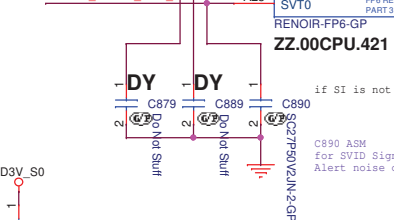
HDMI

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

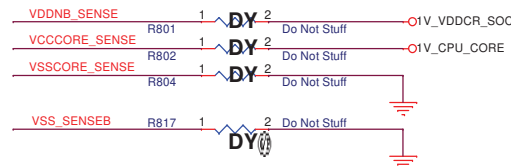
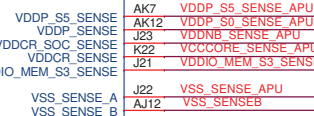
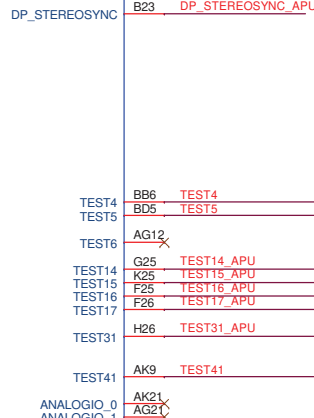
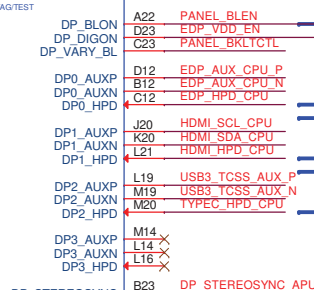
HDT



SVID



CPU1C

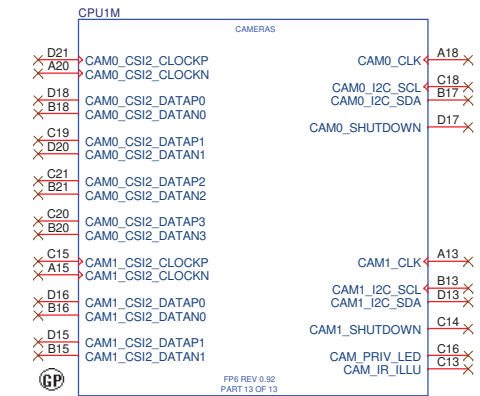
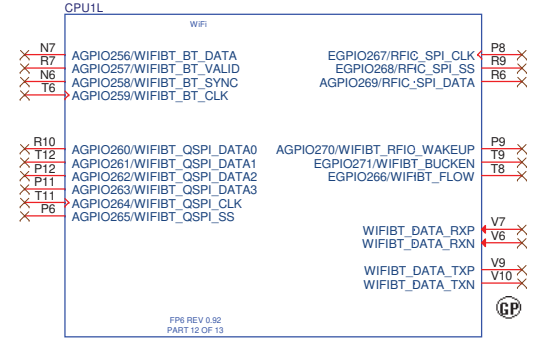
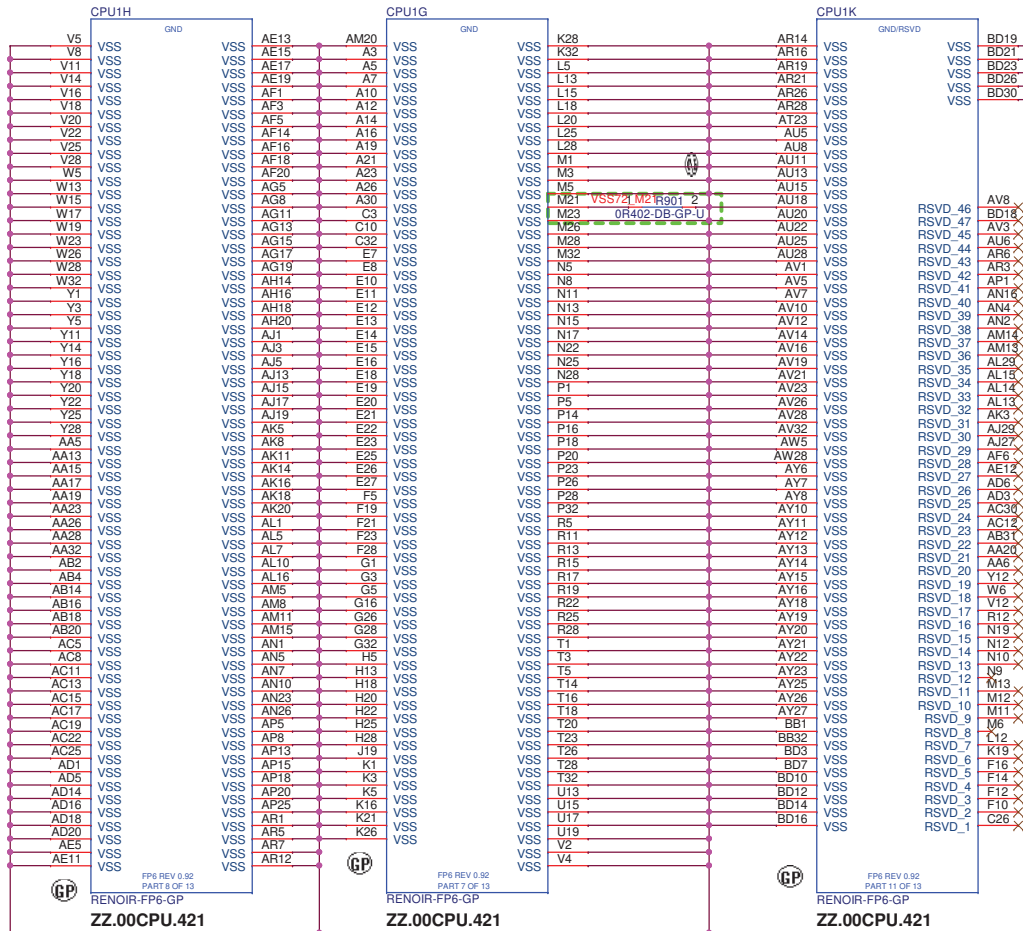


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Title	Document Number	Rev
Size A3	LV550 AMD	SB
Date: Tuesday, April 20, 2021	Sheet 8 of 106	

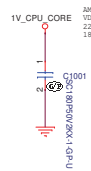
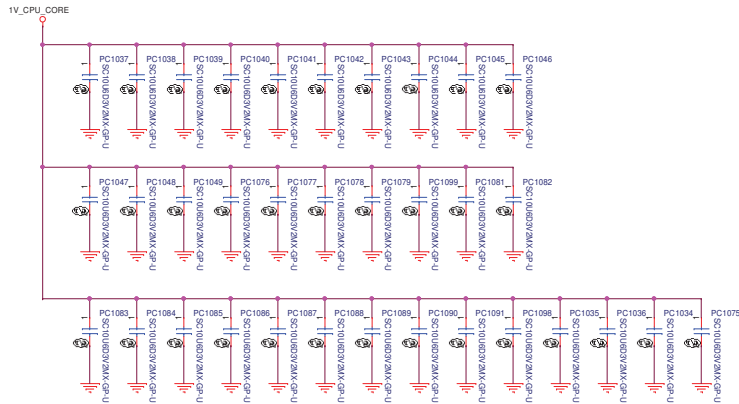
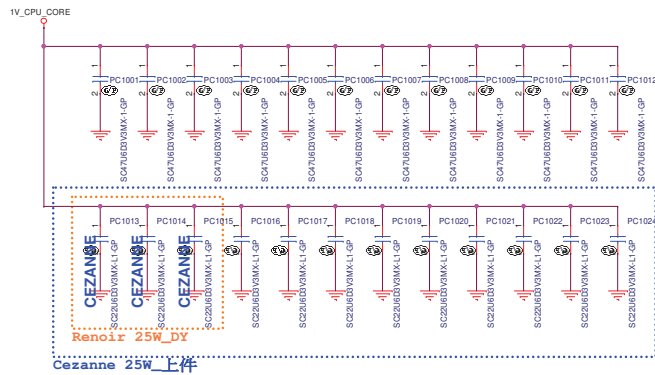
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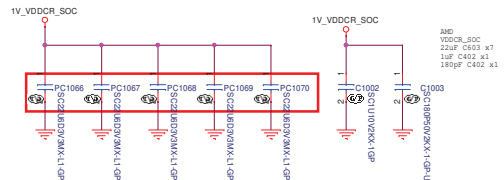
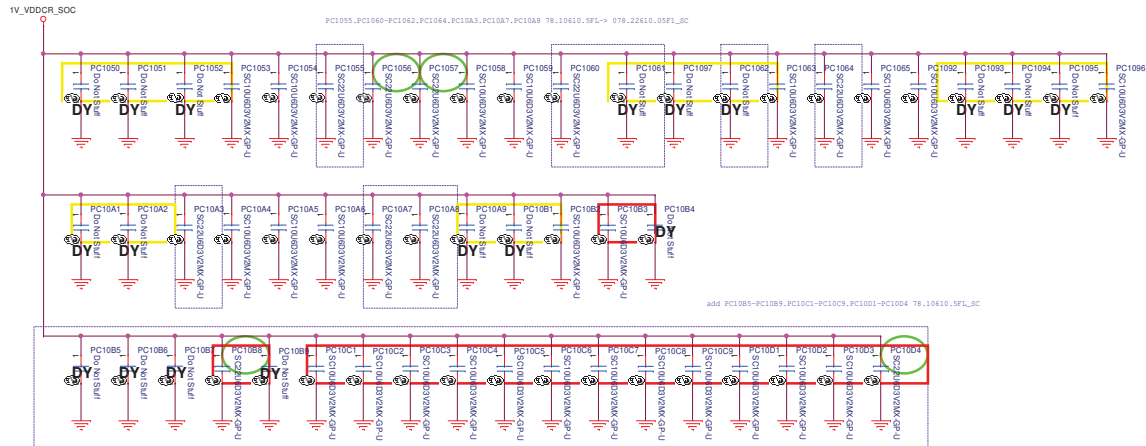
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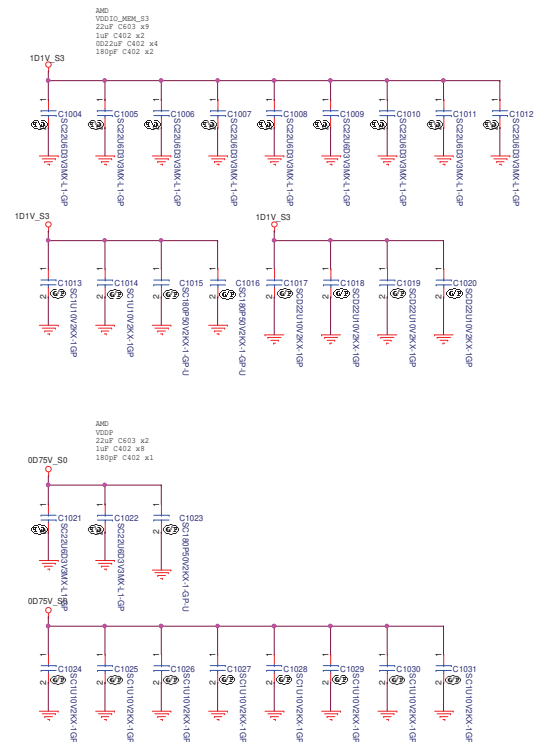
1V_VDDCORE AMD_FP6_25W



1V_VDDCR_SOC



RED:ADM
C1001:078.22610_05P1_3C
GREEN:PC1088 PC1094 PC1095 PC1097 078.22610_05P1_3C (22uF/400V)
20200429_3C



LV550AC

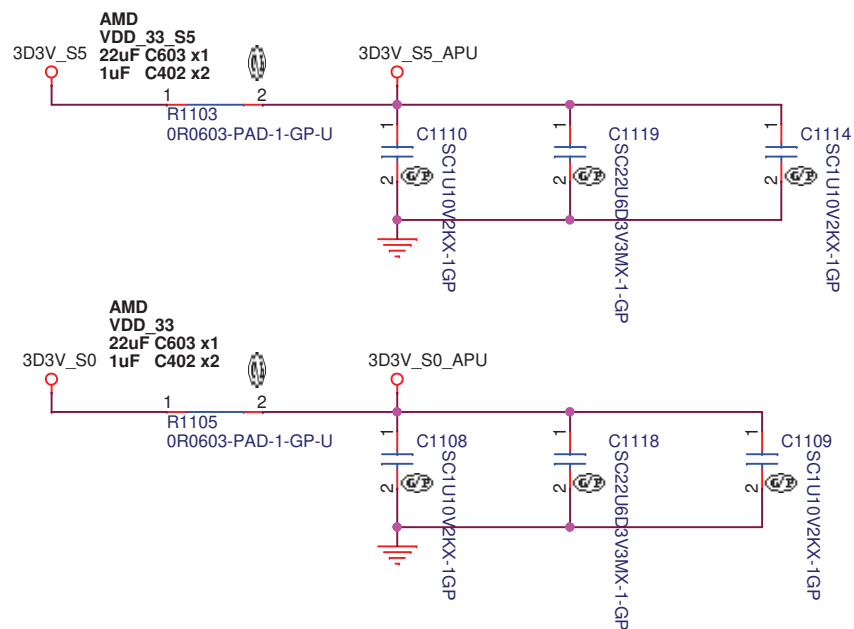
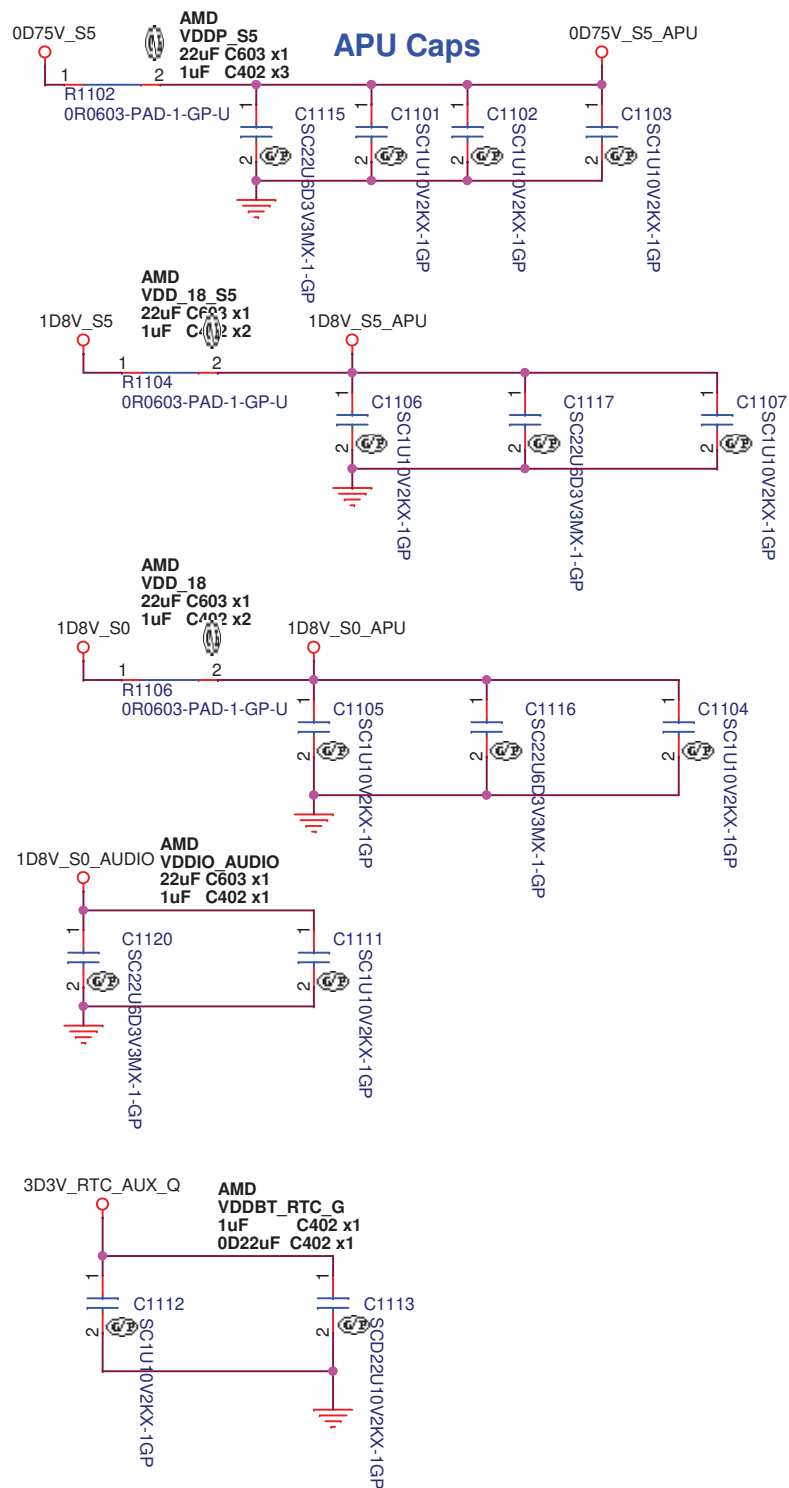


Table 110. Decoupling Capacitors for Processor Power

Capacitor		VDDCR	VDDCR_SOC	VDDIO_MEM_S31 ²	VDDP	VDDP_S5	VDD_18	VDD_18_S5	VDD_33_S5	VDD_33	VDDIO_AUDIO	VDDBT_RTCC_G
Value	Package Size / Material											
22 μF	0603 X5R	16BU	7BU	9BU	2BO	1BO	1BO	1BO	1BO	1BO	1BO	-
1.0 μF	0402 X5R	-	1BU	2BU	4BU + 4BO	2BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU + 1BO	1BU	1BU
0.22 μF	0402 X5R	-	-	4(split)	-	-	-	-	-	-	-	1BU
180 pF	0402 C0G NP0	1BU	1BU	1BU + 2(split)	1BU	-	-	-	-	-	-	-

LV550AC

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Size

Document Number

LV550 AMD

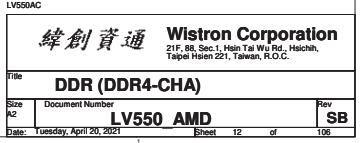
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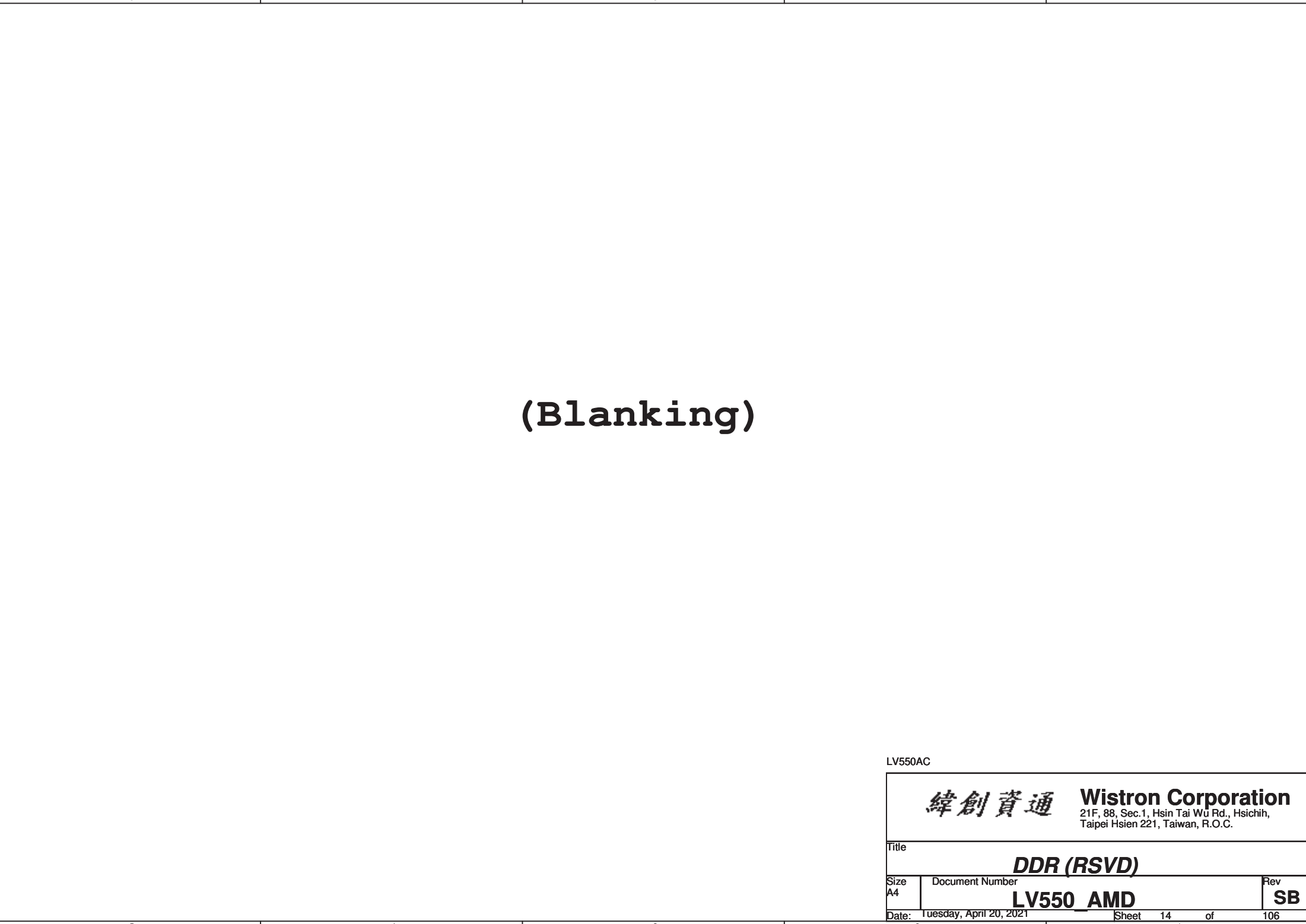
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Sheet 11 of

106






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Title <div>DDR (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
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FCH (RSVD)			
Size	Document Number		Rev
A4	LV550_AMD		SB
Date:	Tuesday, April 20, 2021		Sheet 15 of 106

SSD

63	SSD_CLK_CPU_P	
63	SSD_CLK_CPU_N	
63	SSD_CLKREQ_CPU_N	

WLAN

61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N
61 WLAN_CLKREQ_CPU_N

SPI

20,25	SPI_CLK_ROM	↔	—
25	SPI_SO_ROM	↔	—
25	SPI_SI_ROM	↔	—
25	SPI_WP_ROM	↔	—
25	SPI_HOLD_ROM	↔	—
25	SPI_CS_ROM_N0	↔	—

LPC

24	ECSMI_N_KBC	>>>
24,68	LPC_AD_CPU_P0	>>>
24,68	LPC_AD_CPU_P1	>>>
24,68	LPC_AD_CPU_P2	>>>
24,68	LPC_AD_CPU_P3	>>>
24	LPC_CLK_KBC	>>>
68	LPC_CLK_DBG	<<<
24,68	LPC_SERIRQ_CPU	>>>
24,68	LPC_FRAME_N_CPU	>>>
24,68,91	LPC_RST_N	<<<

24	CLK_RUN_N	
91	PIRQA_N	

24 ECSCI_N_KBC >>_____

```
61 SUS_CLK_CPU <<-----
```

```

91    SPI_CS_CPU_N2
91    SPI_CLK_CPU
91    SPI_SI_CPU
91    SPI_SO_CPU

```

```

68 EC_SMI_APU
68 EGPIO141_RX
68 EGPIO143_TX

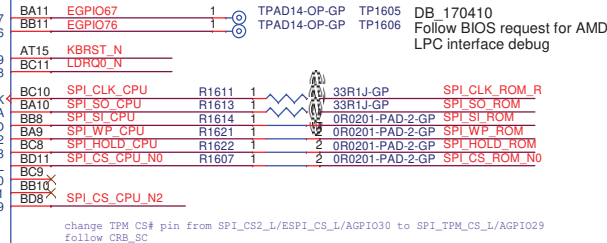
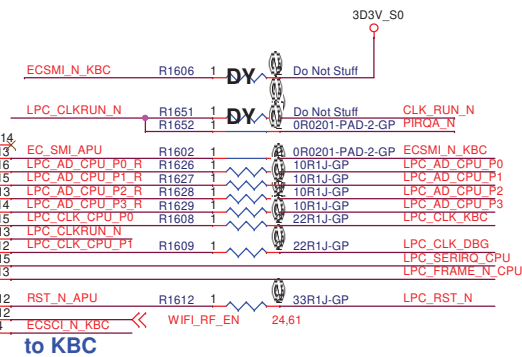
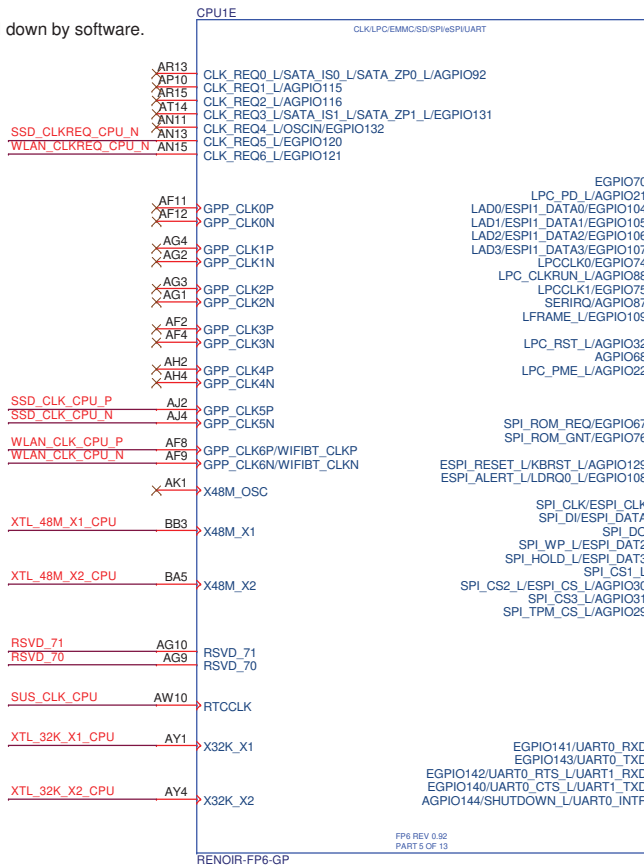
```

CLK/SATA/USB/SPI/LPC

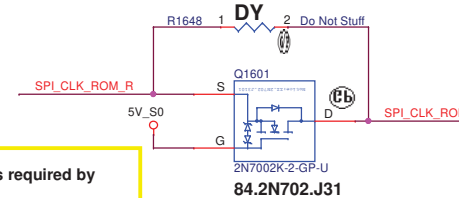
P	GPP CLK port	AMD	Device
0		GFX	NC
1		LAN	NC
2		WWAN	NC
3		PCIETBT	NC
4		PCIEDT	CARD
5		SSD	SSD
6		WLAN	WLAN

LPCCLK1/EGPIO75
CLK_REQ5_L
If unused,
enable internal pull up or pull down by software.

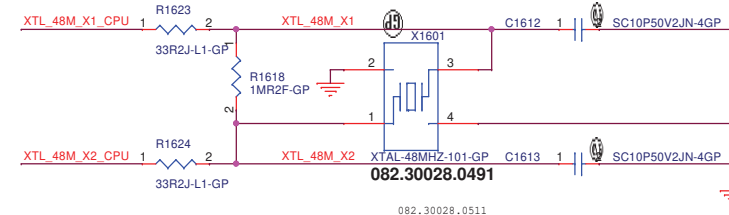
GFX & GPP CLK, 85Ω
SATA & USB, 90Ω



```
change 111 CS_1 path from $11_CS2_2/$11_CS_2/$11_CS_1 CS_1 to $11_CS2_2/$11_CS_2/$11_CS_1
follow CRB_SC
```



Note:
Connected to 48-MHz Fundamental XTAL (± 10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X2.
Connected to 48-MHz Fundamental XTAL (± 10 PPM) with a capacitor to GND as required by XTAL (typically 22 pF) and 1-M ohm 5% resistor to X48M_X1.



082,30028,051

XTAL 32K_X1_CPU R1649 1 2 XTAL 32K_X1 33R2J-L1-GP

XTAL 32K_X2_CPU R1650 1 2 XTAL 32K_X2 33R2J-L1-GP

R1615 1 20MR2J-GP

X1602

XTAL-32D768KHZ-98-GP

082.30003.0301

C1601

SC15P50V2JN-2-GP

C1602

SC15P50V2JN-2-GP

78.15034.1FLLL is common part, but not in stock

<div> <div>V</div> <div>無交期</div> <div>V</div> <div>無交期</div> </div>		C1601	C1602	
	SEIKO 082.30003.0301	15pF	15pF	42A.0M501.0001
	EPSON 082.30003.0191	15pF	15pF	42A.0M501.0002
	NDK 082.30003.0221	15pF	15pF	42A.0M501.0003
	TKC 082.30003.0231	15pF	15pF	42A.0M501.0004
	TAITEN 082.30003.0A11	12pF	12pF	42A.0M501.0005

HARMONY 82.30026.371-> HOSONIC 082.30028.0491 Need 10ppm		
	C1612	C1613
HOSONIC 082.30028.0491 E3FB48E00000VE	10pF	10pF
HOSONIC 082.30028.0511 E3SB48E00000GE		

LV550AC

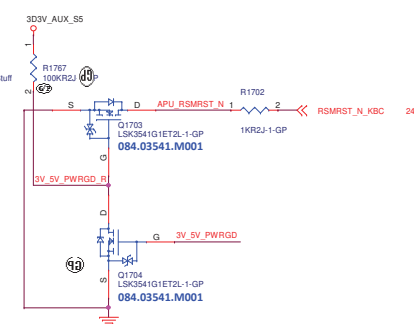
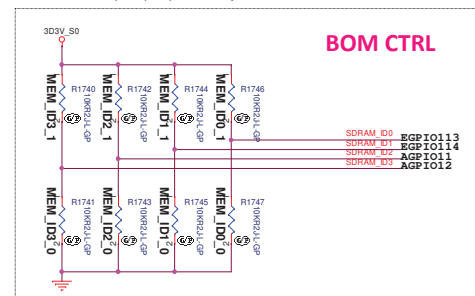
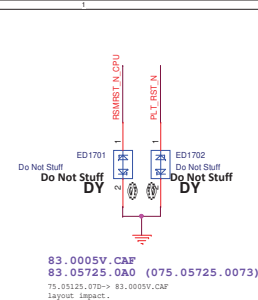
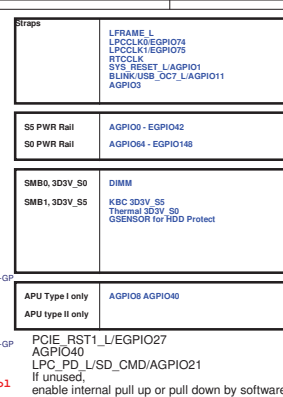
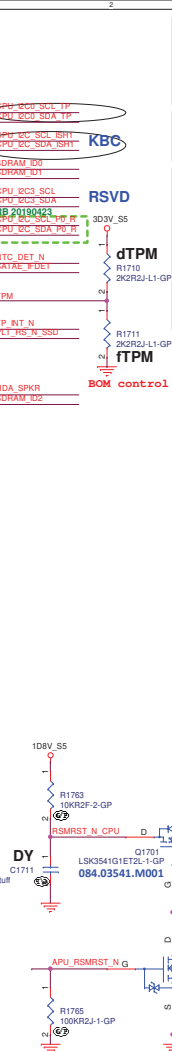
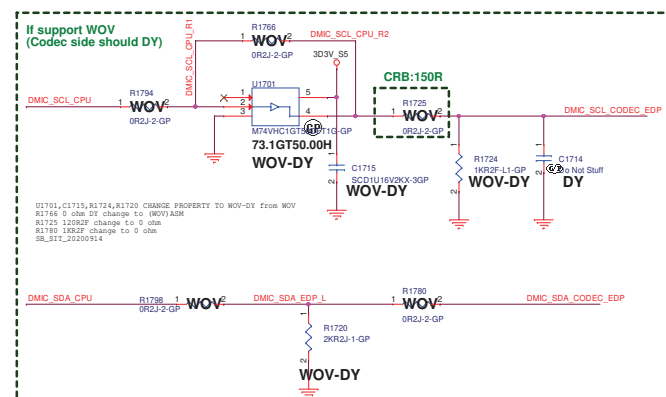
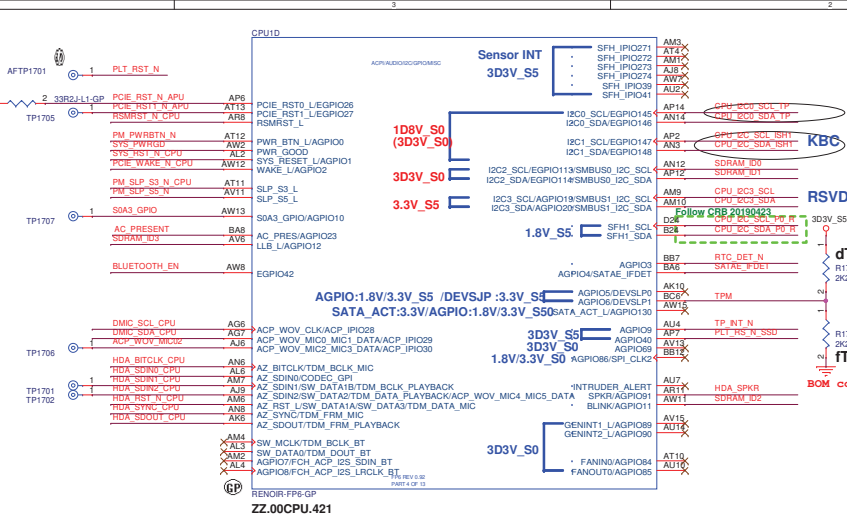
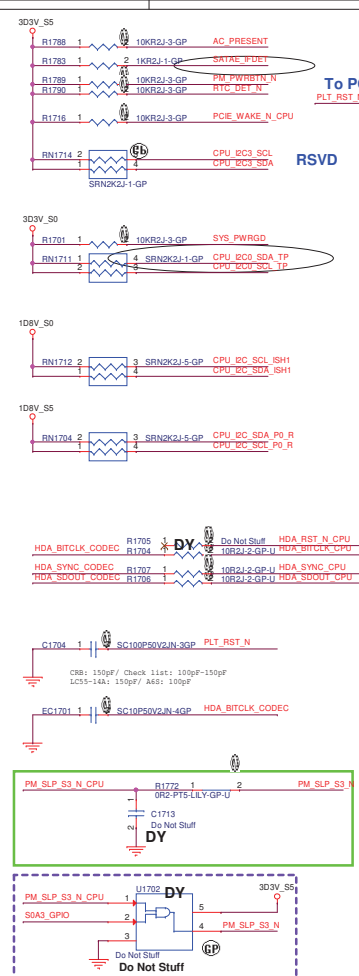
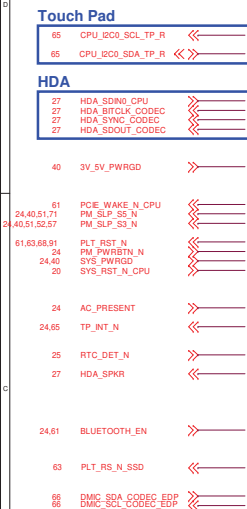
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **ECH (CI K/I PC/SPI/EMMC/SD/LIA)**

Size A3	Document Number LV550 AND	Rev S
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Date: Tuesday, April 20, 2021 Sheet 16 of 106

SSID = PCH
CLK/SATA/USB/SPI/LPC

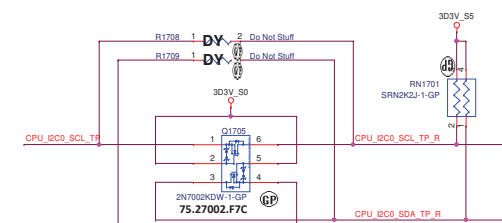


INTERNAL DEBUG PURPOSE ONLY

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

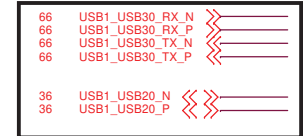
EVT/PVT/SIT/SVT:									
Memory Configuration		Memory Supplier							
00: (Reserve) 01: 8GB 10: 16GB 11: (Reserve)		00: Samsung 01: Micron 10: SK Hynix 11: (Reserve)							
AGPIO12	AGPIO11	EGPIO114	EGPIO113	Agpio12	Agpio11	Supplier	Density	PN	
0	1	0	0	0	0	SAMSUNG	8GB	SM30N76677	10*15 mm
1	0	0	0	0	0	SAMSUNG	16GB	SM30N76678	10*15 mm
1	1	1	1	1	1	SAMSUNG	8GB	SM30N76677	10*15 mm
0	1	0	1	0	1	MICRON	8GB	SM30E1328	10*14.5 mm
1	0	0	1	1	0	MICRON	16GB	SM30N76681	10*14.5 mm
0	1	1	0	0	1	SK HYNIX	8GB	SM30N76602	10*15 mm
1	0	1	0	1	0	SK HYNIX	16GB	SM30N76603	10*15 mm
0	1	1	0	0	1	SK HYNIX	8GB	SM30N76602	10*15 mm

0=L, 1=H

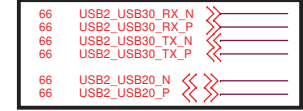


Main Func = USB

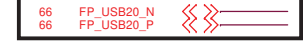
USB3.0 Port1



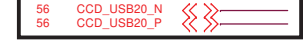
USB3.0 Port2



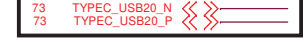
Finger Printer



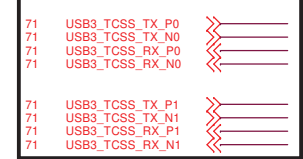
IR Camera



Type C USB20



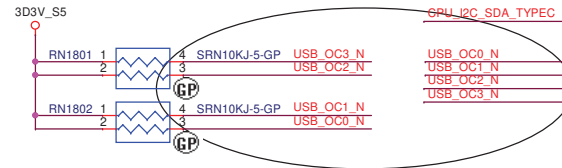
Type-C



BT



USB_OC0#	USB3.0 Power
USB_OC1#	USB3.0 Power
USB_OC2#	Type C
USB_OC3#	N/A



Type-C

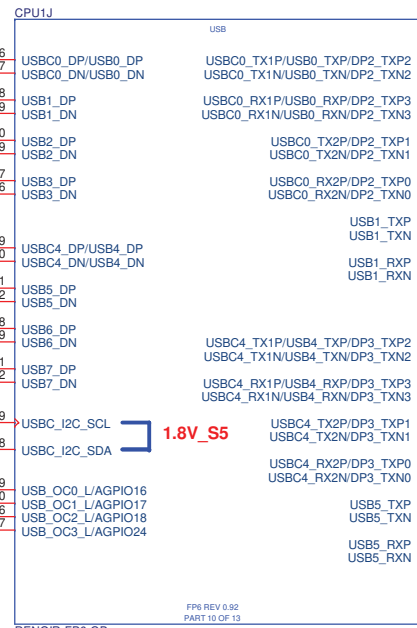
USB2.0 Port1

Camera

USB2.0 Port5

Finger Printer RSVD

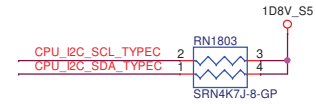
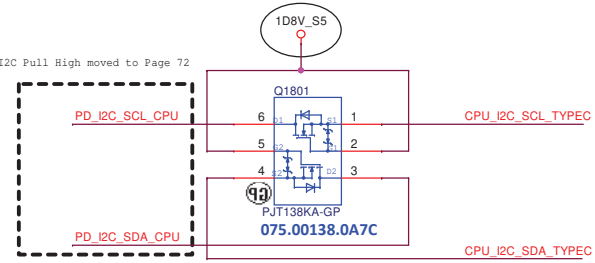
BlueTooth



RENOIR-FP6-GP
ZZ.00CPU.421

AGPIO13/USB_OC5_L
If unused,
enable internal pull up or pull down by software.

PD I2C Pull High moved to Page 72



LV550AC

(Blanking)

LV550AC

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

FCH (RSVD)

Size
A4

Document Number

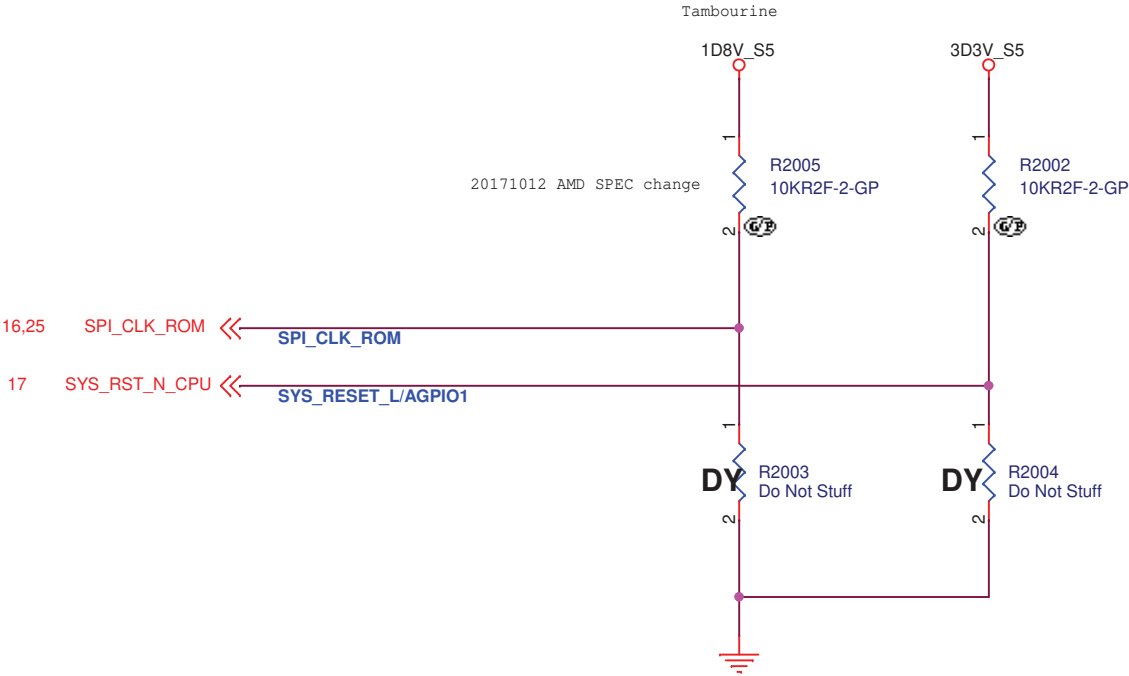
LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 19 of 106

STRAP PINS



	PIN SPI_CLK NET SPI_CLK_ROM	PIN SYS_RESET_L//AGPIO1 NET SYS_RST#_CPU
PULL HIGH	Configured for internal clock-generator 10kΩ(± 5%) pull-up resistor to VDD_18 (DEFAULT)	Normal powerup / reset timing 10kΩ(± 5%) pull-up resistor to VDD_33_S5 (DEFAULT)
PULL LOW	Reserved	Reserved

LV550AC

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Title

FCH (Strap)

Size
A4

Document Number
LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 20 of 106

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LV550AC		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
FCH (RSVD)		
Size	Document Number	Rev
A4	LV550_AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 21 of 106

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LV550AC

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **FCH (RSVD)**

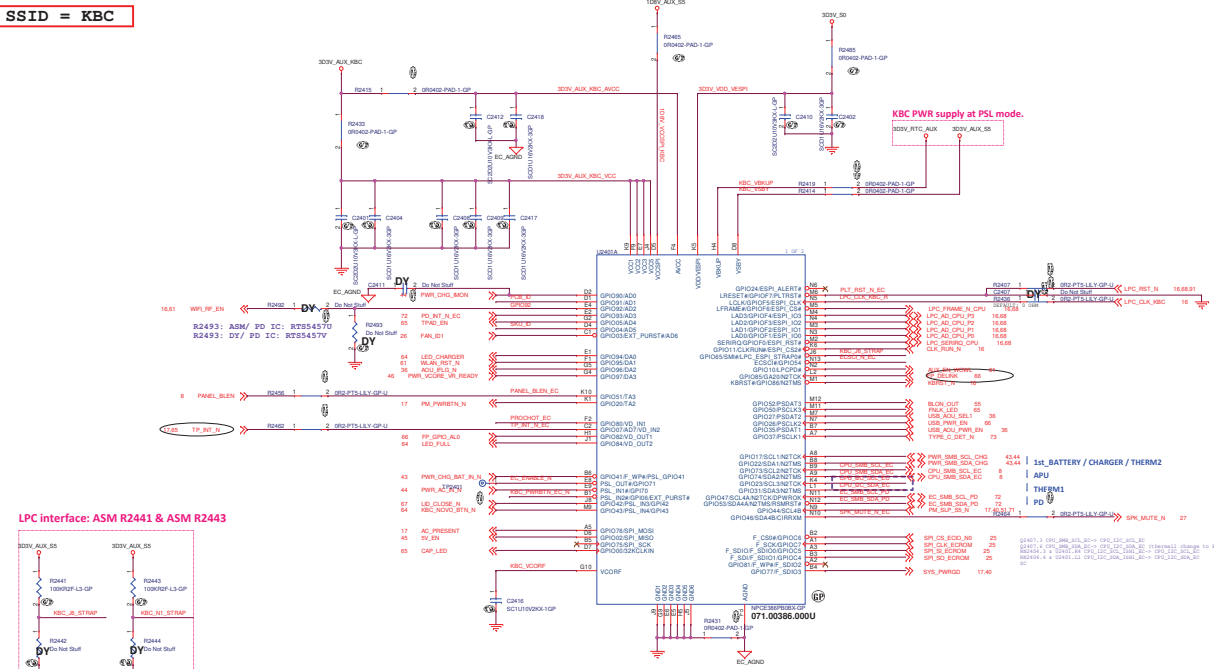
Size A4	Document Number LV550_AMD	Rev SB
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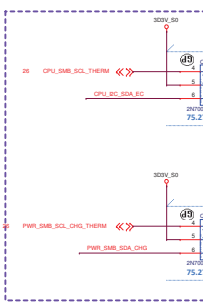
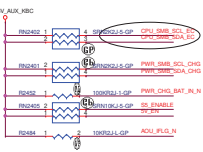
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LV550AC			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (RSVD)			
Size	Document Number		Rev
A4	LV550_AMD		SB
Date: Tuesday, April 20, 2021		Sheet 23 of	106

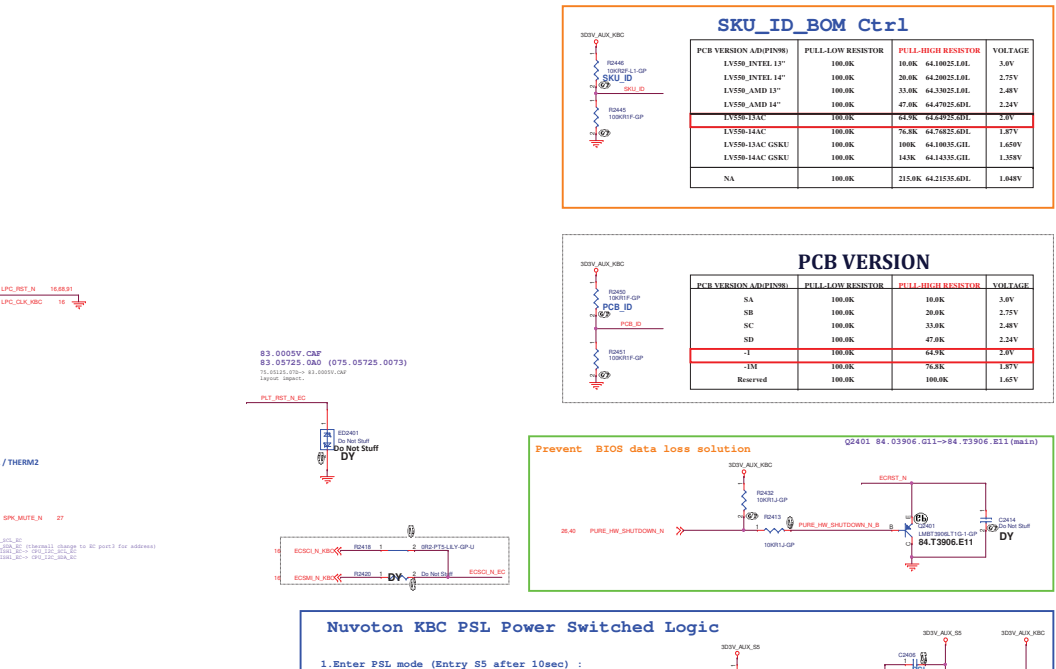
SSID = KBC



EC GPIO PH



SSID = KBC

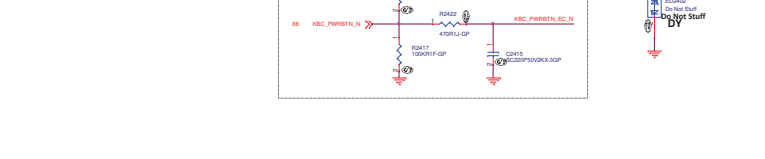
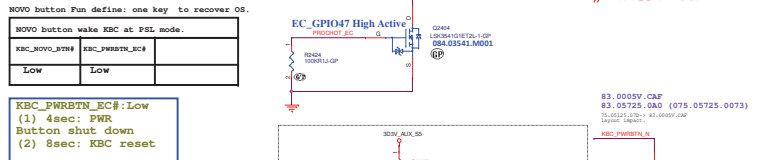
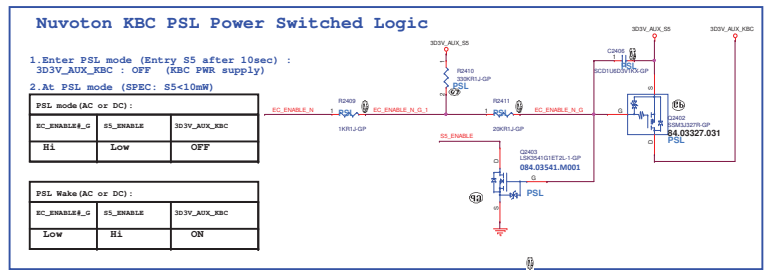
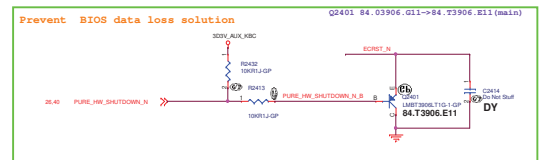


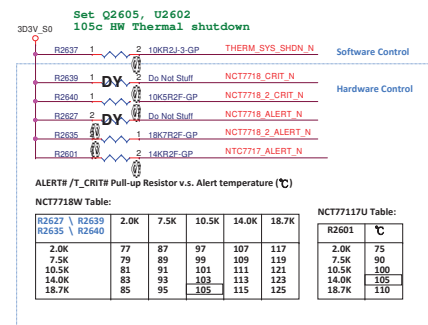
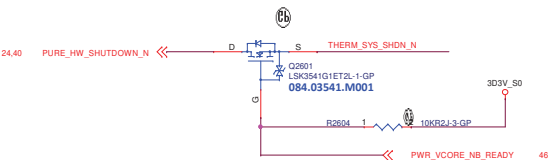
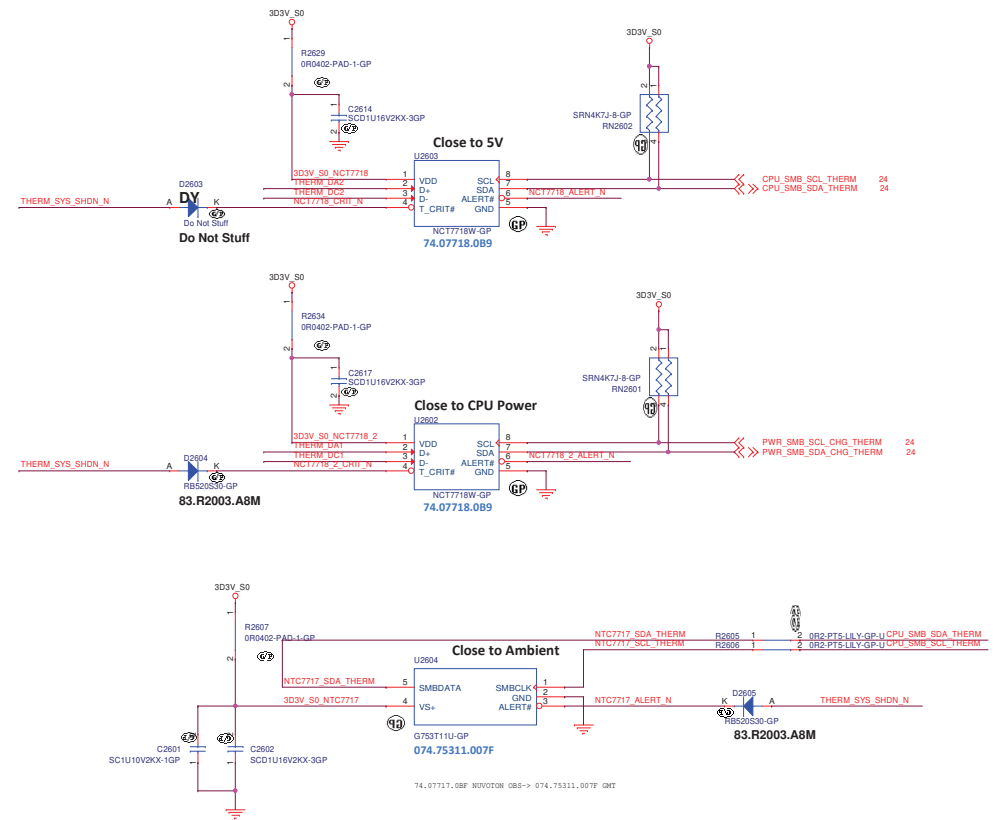
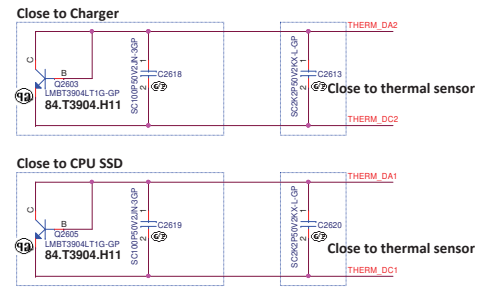
EC GPIO PH



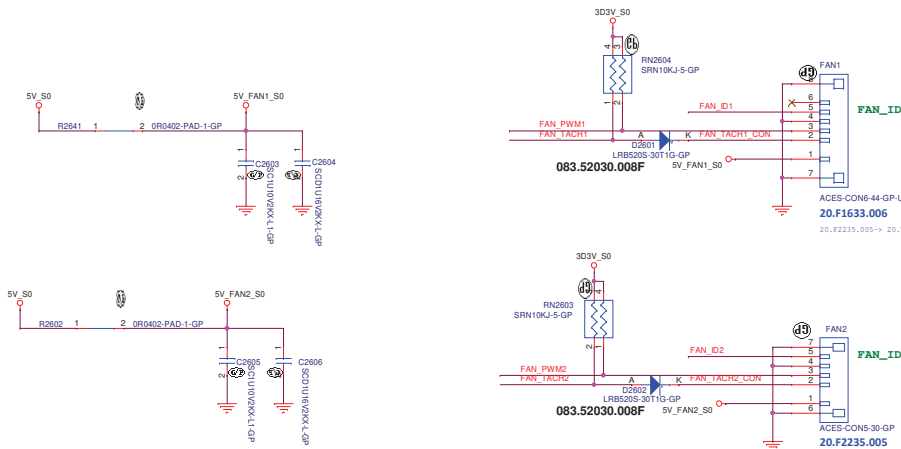
SKU_ID_BOM Ctrl1				
PCB VERSION	ADP/PINNO	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
LV550_INTEL_13"	100.0K	10.0K	64.38025.1.0L	3.8V
LV550_INTEL_14"	100.0K	20.0K	64.38025.1.0L	2.75V
LV550_AMD_13"	100.0K	33.0K	64.38025.1.0L	2.48V
LV550_AMD_14"	100.0K	47.0K	64.38025.1.0L	2.24V
LV550-13UC	100.0K	64.3K	64.38025.1.0L	2.8V
LV550-14AC	100.0K	76.3K	64.38025.1.0L	1.87V
LV550-13AC GSKU	100.0K	100K	64.38025.1.0L	1.60V
LV550-14AC GSKU	100.0K	143K	64.38025.1.0L	1.58V
NA	100.0K	215.0K	64.21535.1.0L	1.04V

PCB VERSION				
PCB VERSION	ADP/PINNO	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	10.0K	3.8V
SB	100.0K	20.0K	20.0K	2.75V
SC	100.0K	33.0K	33.0K	2.48V
SD	100.0K	47.0K	47.0K	2.24V
-1	100.0K	64.3K	64.3K	2.8V
-1M	100.0K	76.3K	76.3K	1.87V
Reserved	100.0K	100.0K	100.0K	1.65V

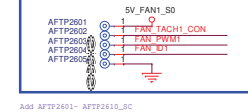




24 FAN_TACH1
24 FAN_TACH2
24 FAN_PWM1
24 FAN_PWM2
24 FAN_ID1
24 FAN_ID2



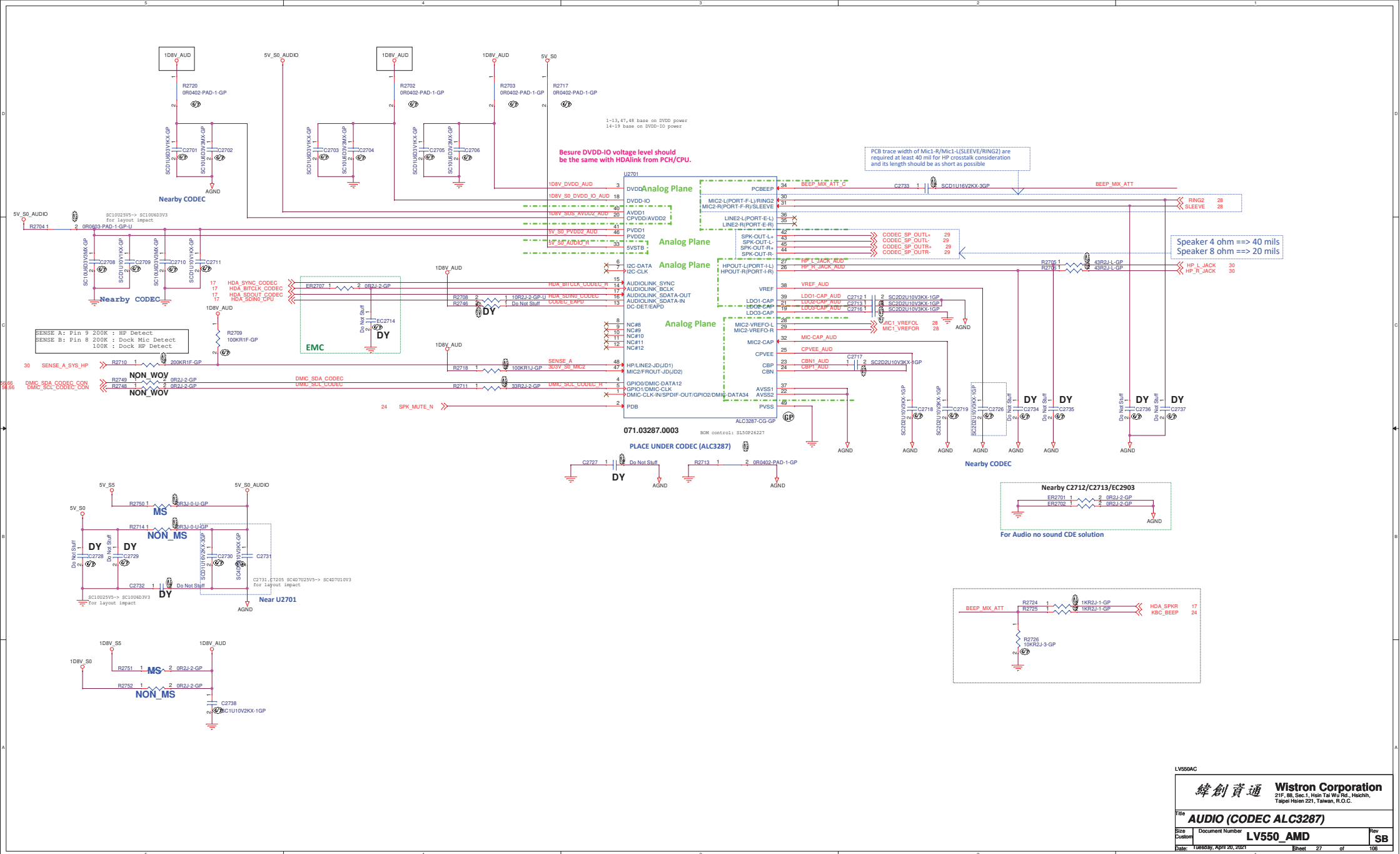
Test point-Top

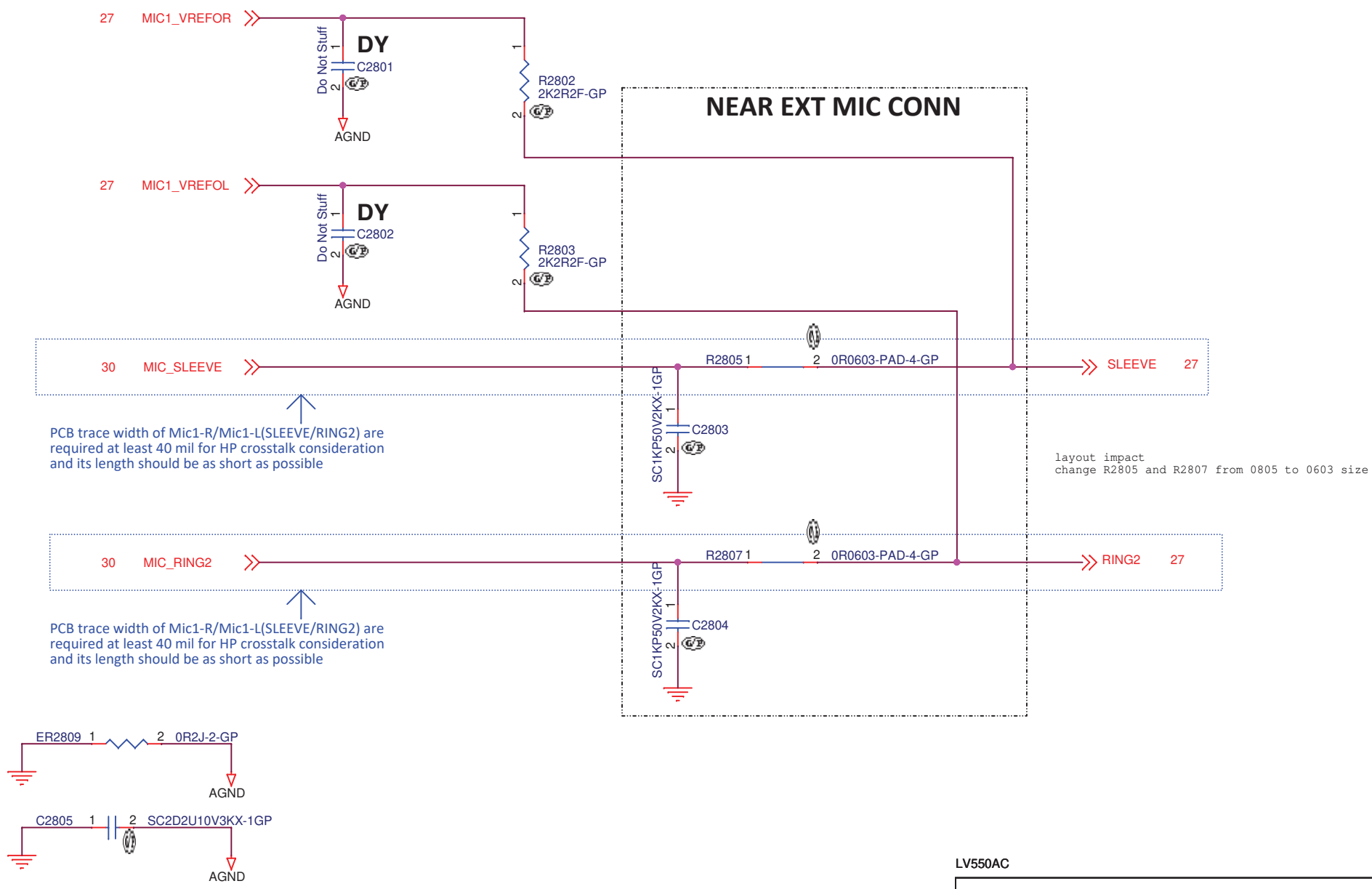


Test point-Top



LV550AC

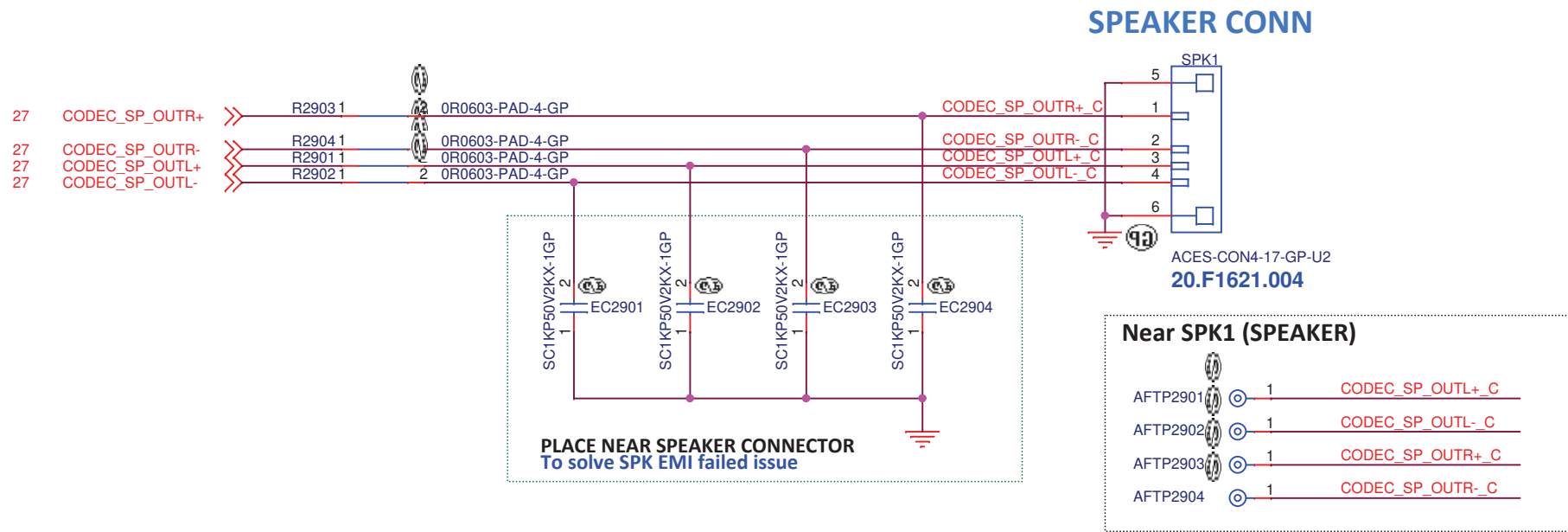




LV550AC

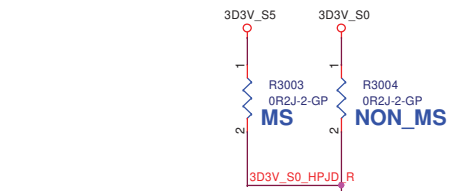
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO (MIC I/F)			
Size A4	Document Number LV550_AMD		Rev SB
Date:	Tuesday, April 20, 2021	Sheet 28 of	106

Main Func = AUDIO



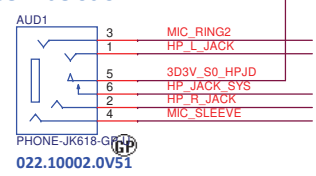
LV550AC

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title AUDIO (SPEAKER)			
Size A4	Document Number LV550_AMD		Rev SB
Date: Tuesday, April 20, 2021		Sheet 29	of 106

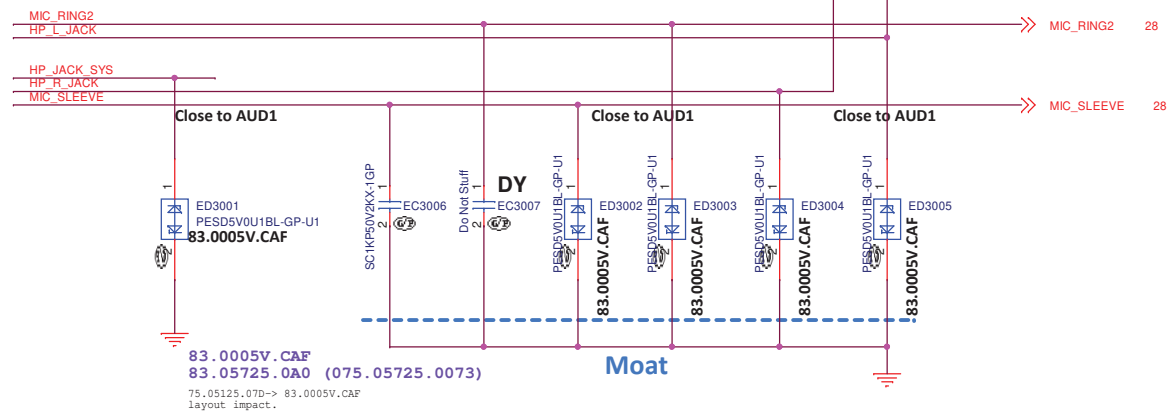
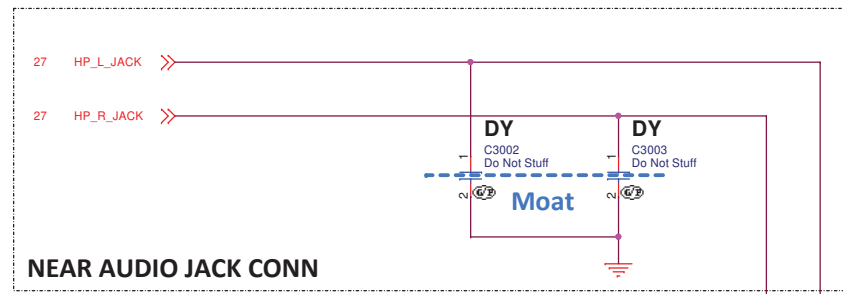
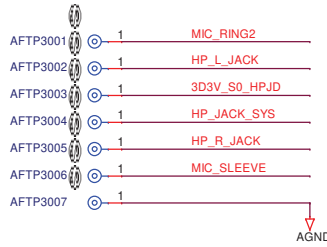


022.10002.0D21-> 022.10002.0P31
-> 022.10002.0V51/022.10002.0V21

Combo Jack

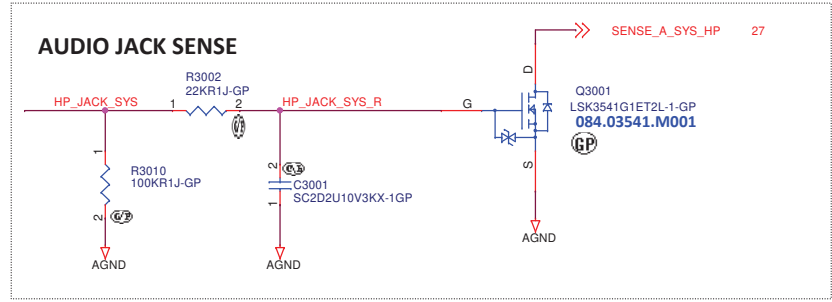


Near AUD1 (AUDIO)

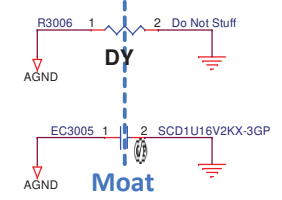


AUDIO JACK SENSE

CLOSE TO CODEC
6-10 mil trace recommend



HGND A/HGND B trace width >70mil,
changed to sharp will be better.



LV550AC

Title		Wistron Corporation	
Size		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Date		Tuesday, April 20, 2021	
Document Number		LV550_AMD	
Rev		SB	
Sheet		30 of 106	

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LV550AC

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN (RSVD)

Size
A4

Document Number

LV550 AMD

Rev

SB

Date: Tuesday, April 20, 2021

Sheet 31 of 106

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LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 32 of 106

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(Blanking)

LV550AC

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>CARD READER (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 33 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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LV550AC

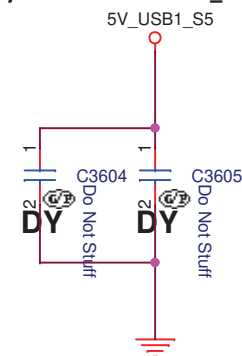
緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
USB (RSVD)					
Size	Document Number				Rev
A4	LV550_AMD				SB
Date: Tuesday, April 20, 2021			Sheet	34	of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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LV550AC			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (RSVD)			
Size A4	Document Number LV550_AMD		Rev SB
Date: Tuesday, April 20, 2021		Sheet 35 of	106

For USB3.0 System Port1 (For AOU)



Current Limit Target : 2.3A (2.1-2.45A)

TABLE of AOU port: U3601

	Vendor	Vendor P/N	Wistron P/N
1st	TI	SN1702001RTER	SL50Q67167AA
2nd	DIODES	PI5USB2546HZHEX	SL50Q67168AA

SN1702001RTER is not equivalent device of TPS2546RTER

LV550AC

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB(USB Charger)

Size
A4

Document Number

LV550 AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 36 of 106

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>USB (RSVD)(PCIE to USB3.0)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 37 of 106

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LV550AC

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>USB (RSVD)(USB Redriver/Hub)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 38 of 106

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
TitleSequence (RSVD)		
SizeA4	Document NumberLV550_AMD	RevSB
Date: Tuesday, April 20, 2021		Sheet 39 of 106

Power Sequence

17,24,51,52,57 PM_SLP_S3_N >>

17,24,51,71 PM_SLP_S5_N >>_____

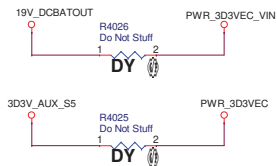
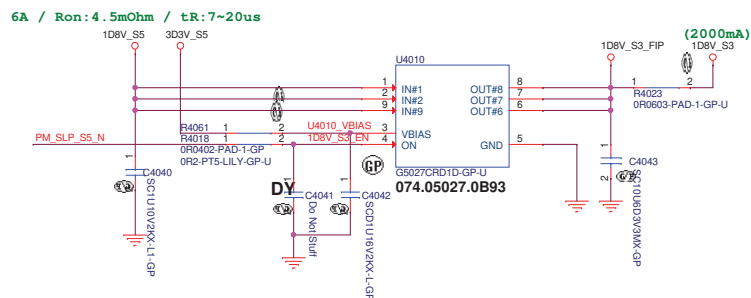
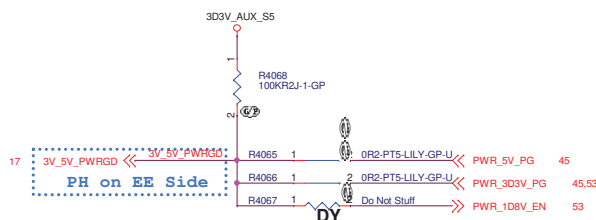
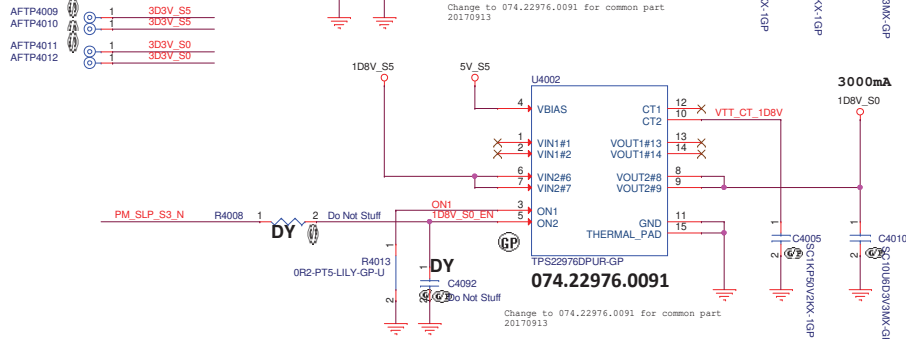
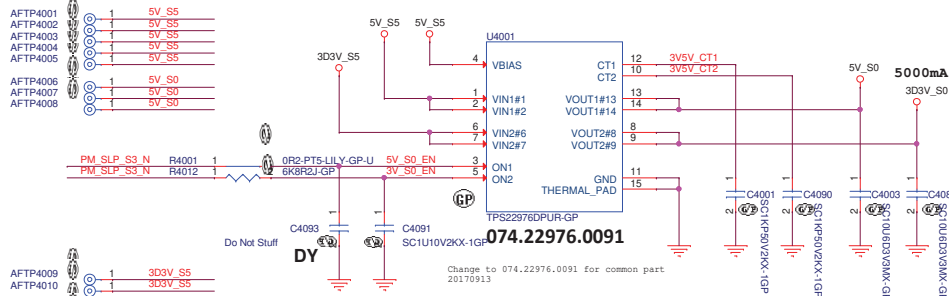
45 3V_5V_EN <<-----

24,26 PURE_HW_SHUTDOWN_N >>————

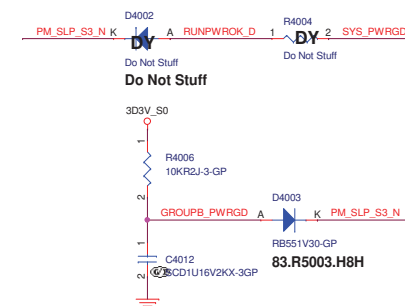
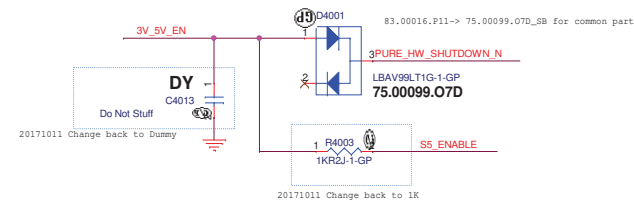
24,45,52,53 S5_ENABLE >>_____

17,24 SYS_PWRGD >>_____

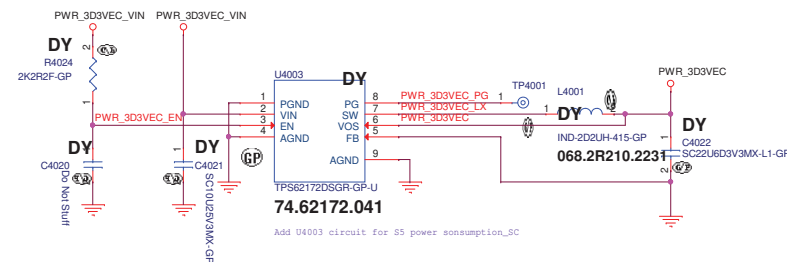
46,52 PWR_VDDPRUN_PG >> R4002 1 2 1D8V_S0_EN



Add U4003 circuit for S5 power consumption_SC



Delay for S0_PWRGD to VCORE_EN



LV550AC

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Sequence (Power Plane Enable)
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Size Custom	Document Number	Rev
	LV550 AMD	SI
Date: Tuesday, April 20, 2021	Sheet 40 of 106	

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Title		
Sequence (RSVD) (DS3/S0ix)		
Size	Document Number	Rev
A4	LV550_AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 41 of 106

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>INT IO (RSVD)(TYPEC DC-DC)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date <div>Tuesday, April 20, 2021</div>		Sheet <div>42</div> of <div>106</div>

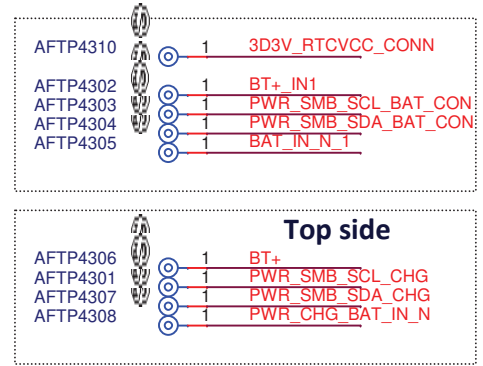
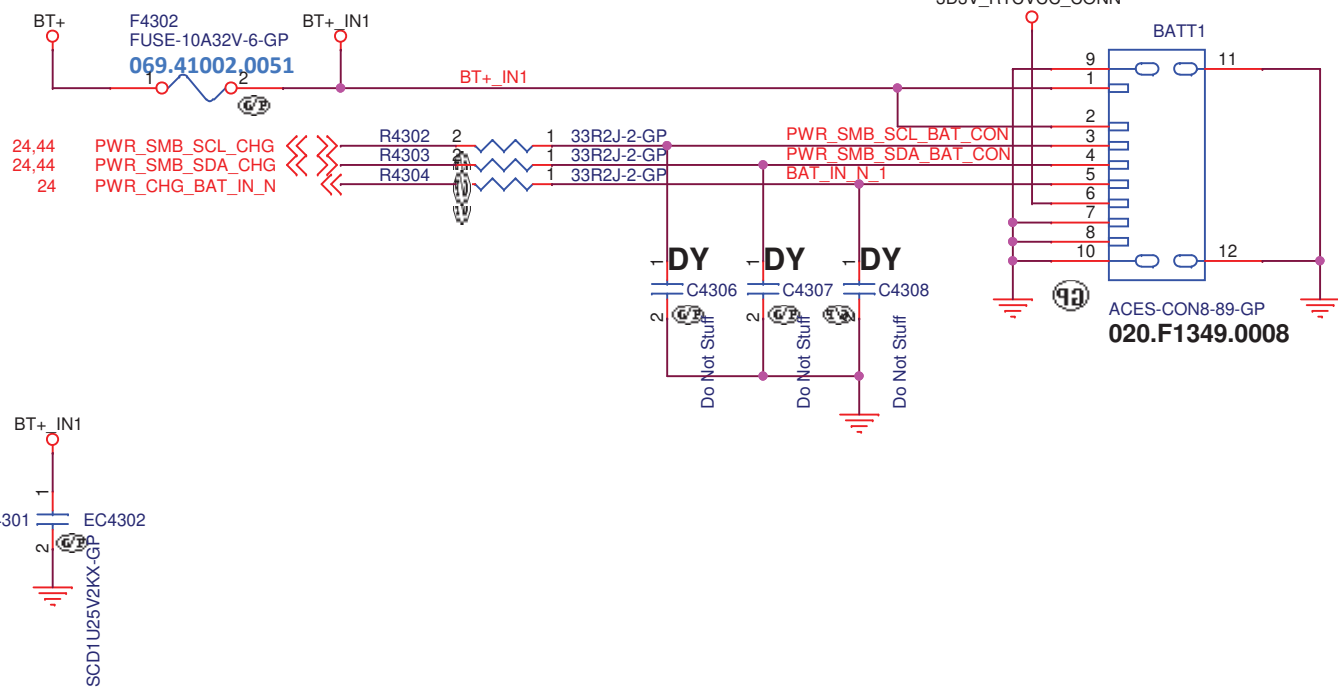
5

4

3

2

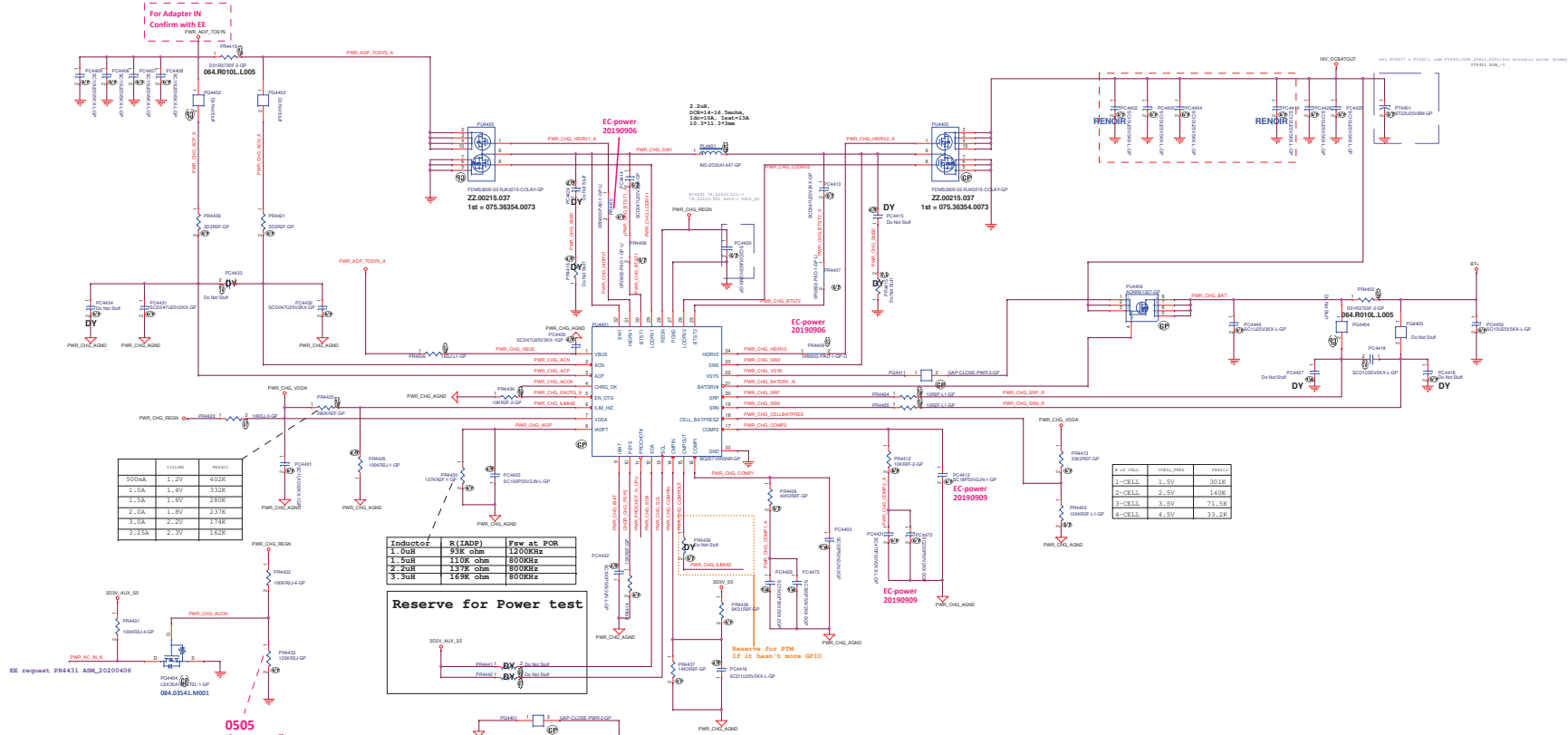
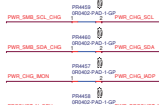
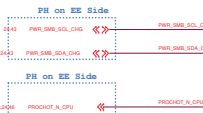
1



LV550AC

緯創資通			Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title INT IO (DCIN/BATT CONN)					
Size A4	Document Number LV550_AMD				Rev SB
Date: Tuesday, April 20, 2021		Sheet	43	of	106

OFFPAGE - PIC - EE



	V (1.0V)	PR6420
500mA	1.2V	402K
1.0A	1.4V	332K
1.5A	1.6V	280K
2.0A	1.8V	237K
3.0A	2.2V	174K
5.0A	3.0V	125K

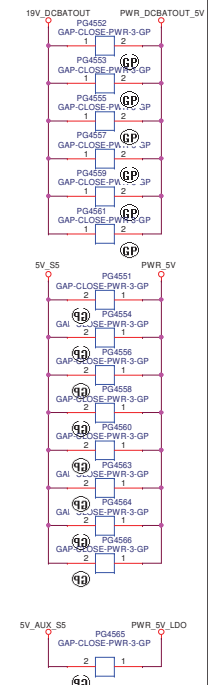
Inductor	R(IADP)	Fsw at POR
1.0uH	93K ohm	1200KHz
1.5uH	110K ohm	800KHz
2.2uH	137K ohm	800KHz
3.3uH	169K ohm	800KHz

Reserve for Power test

0505
buyer: 7'

# of CELL	VCELL_FREE	FRAC
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

OFFPAGE-GAP



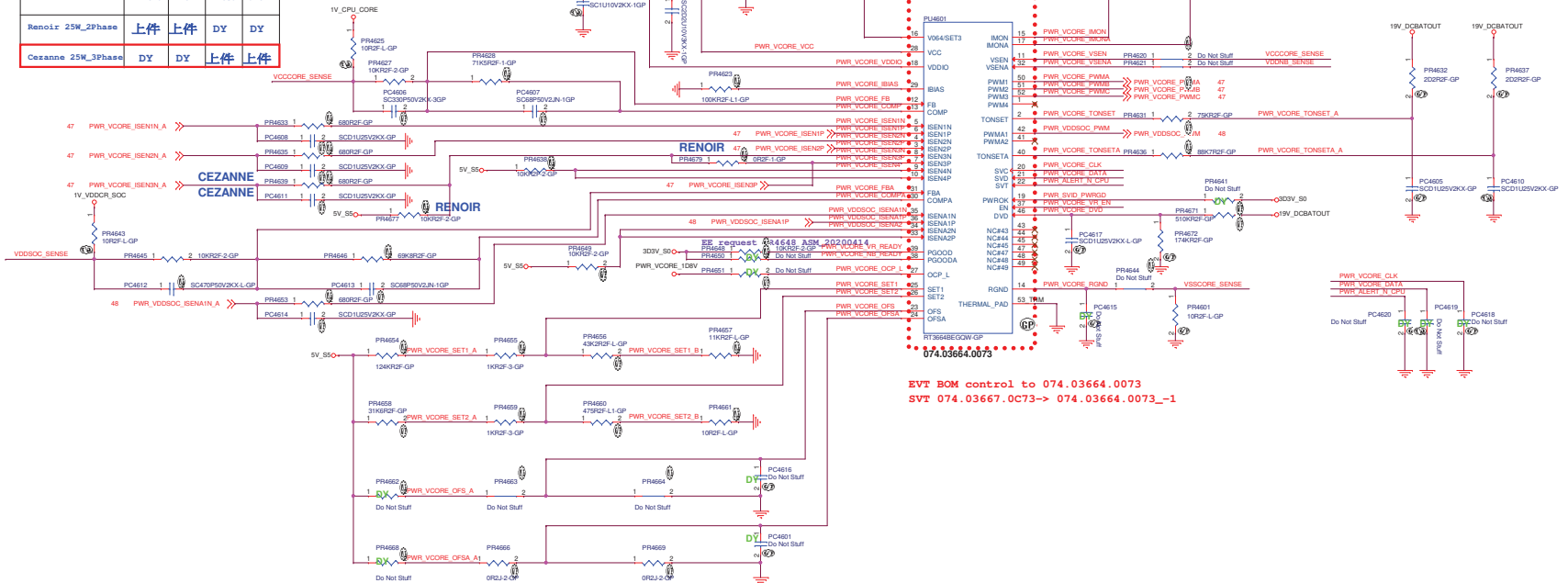
IDC:8A

	PROCHOT_N_CPU	PROCHOT_N_CPU
SVID_ALERT_CPU_N	PR4602 1	PWR_ALERT_N_CPU
SVID_CLK_CPU	PR4603 1	PWR_VCORE_CLK
SVID_DATA_CPU	PR4604 1	PWR_VCORE_DATA
SVID_DATA_CPU	PR4605 1	PWR_VCORE_DATA

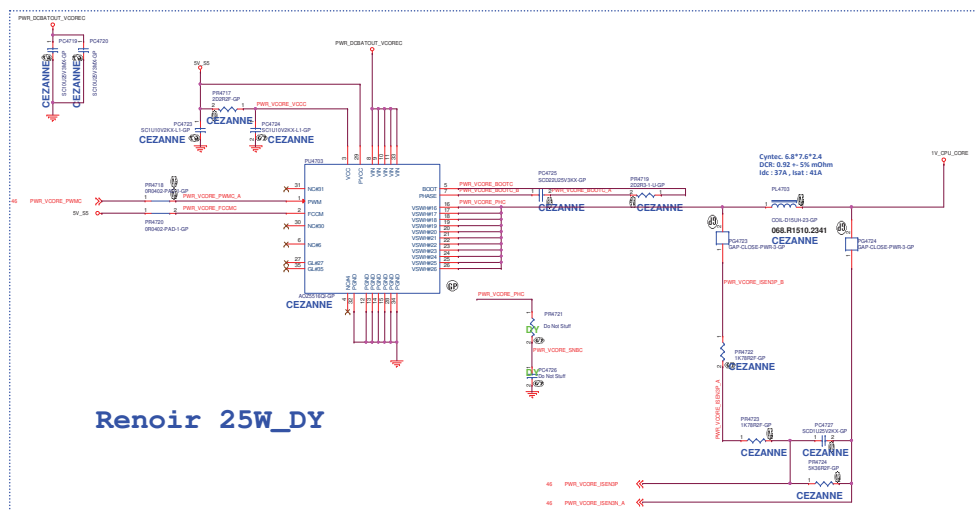
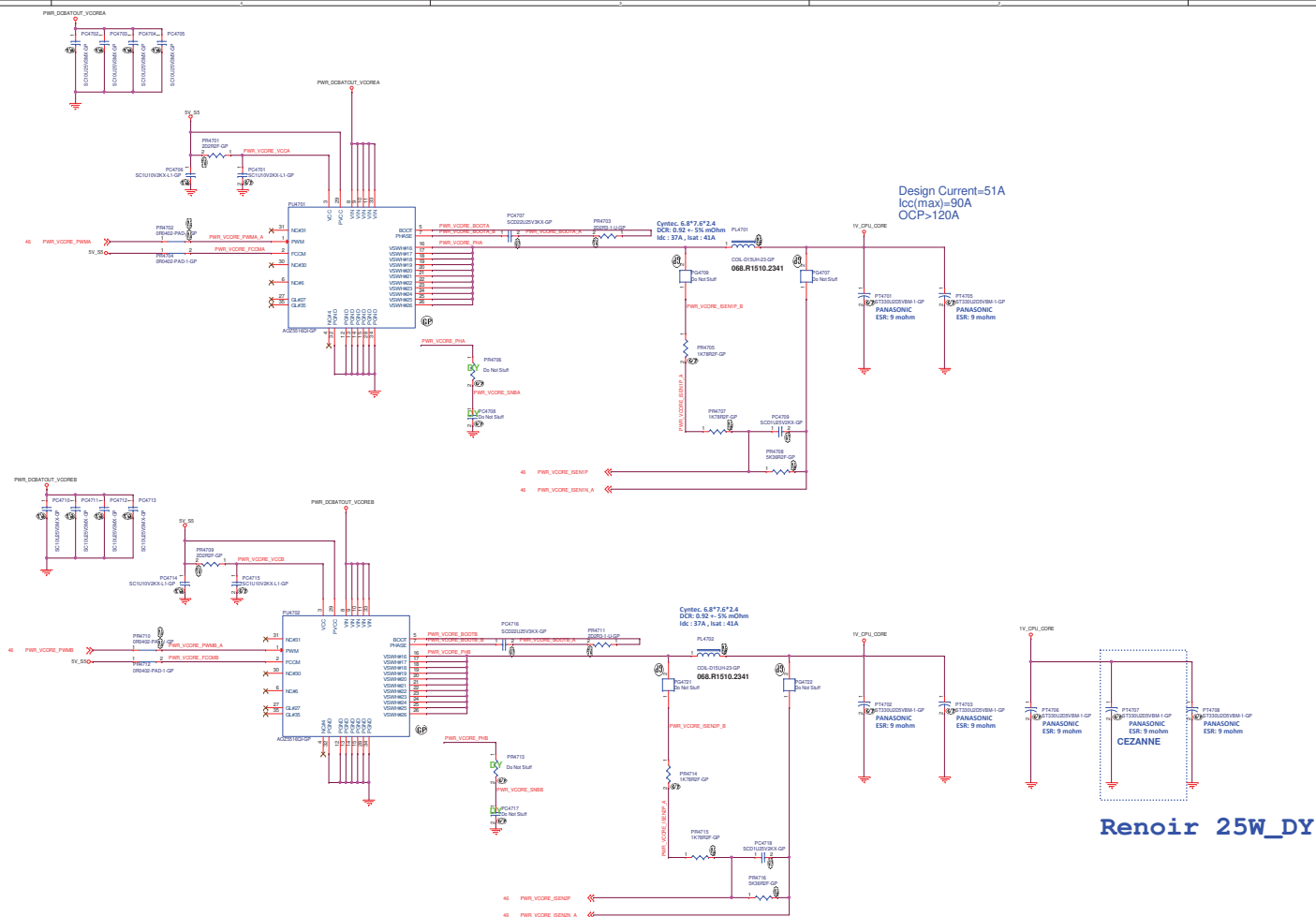
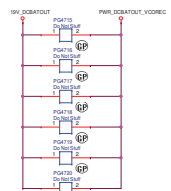
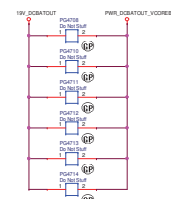
24 PWR_VCORE_VR_READY << PWR_VCORE_NB_READY

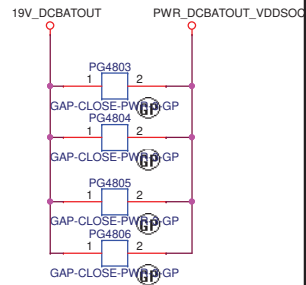


	PR4679	PR4677	PR4639	PC4611
Renoir 25W_2Phase	<u>上件</u>	<u>上件</u>	DY	DY
Cezanne 25W_3Phase	DY	DY	<u>上件</u>	<u>上件</u>

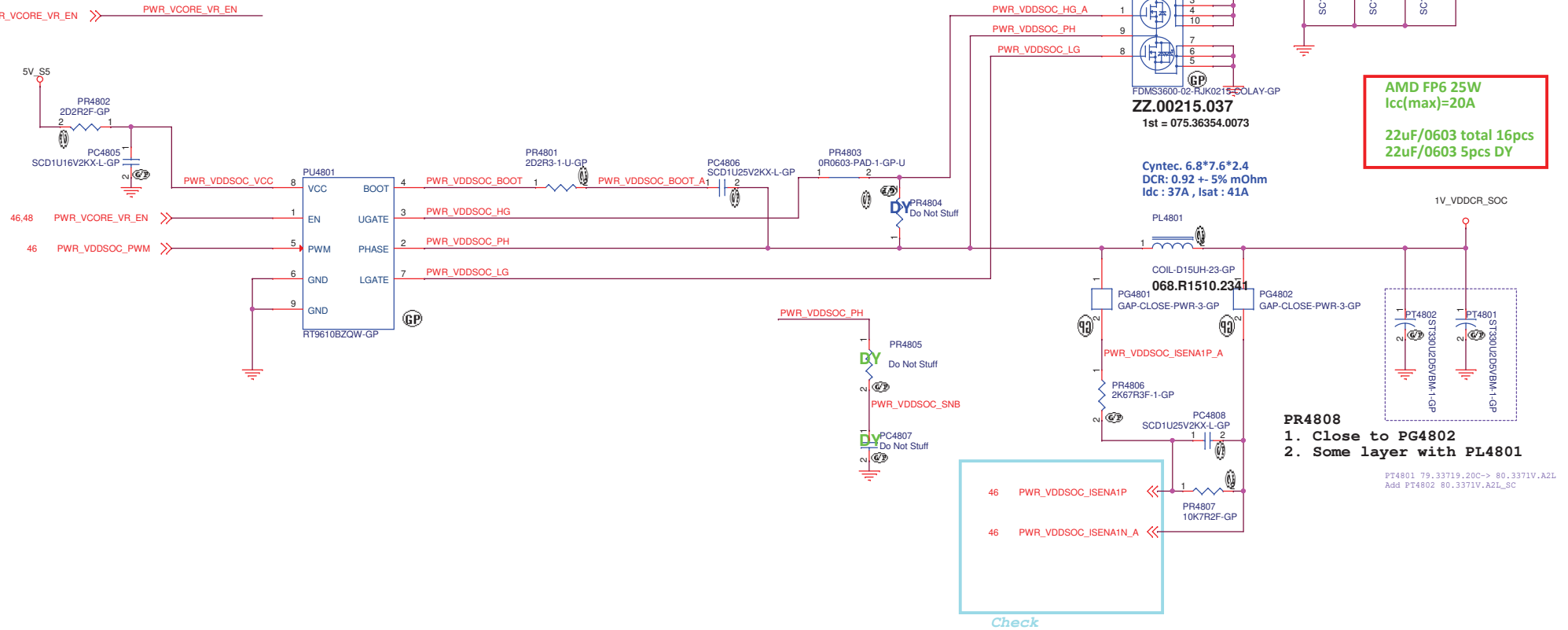


EVT BOM control to 074.03664.0073
SVT 074.03667.0C73-> 074.03664.0073_-1





AMD FP6 35W
Icc(max)=20A
22uF/0603 total 25pcs



LV550AC

緯創資通 Wistron Corporation		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RT9610_VDDSOC(3/3)			
Size Custom	Document Number	Rev SB	
Date: Tuesday, April 20, 2021	Sheet 48 of 106		

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LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 49 of 106

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LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power (RSVD)

Size
A4

Document Number

LV550_AMD

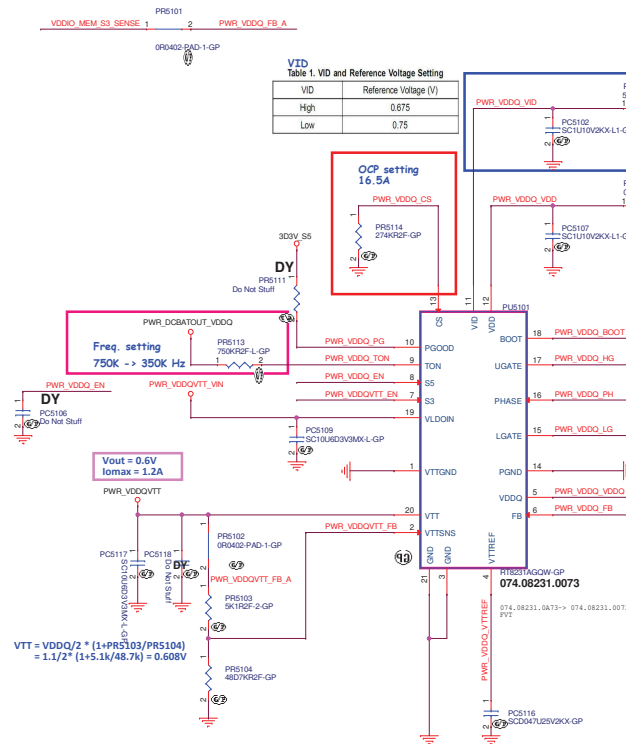
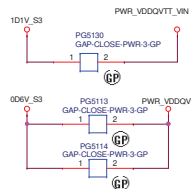
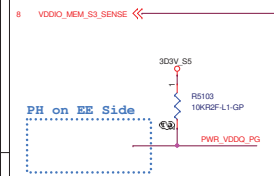
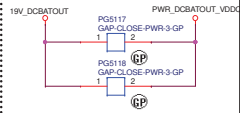
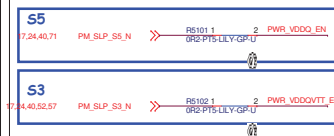
Rev
SB

Date: Tuesday, April 20, 2021

Sheet 50 of 106

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OFFPAGE_GAP

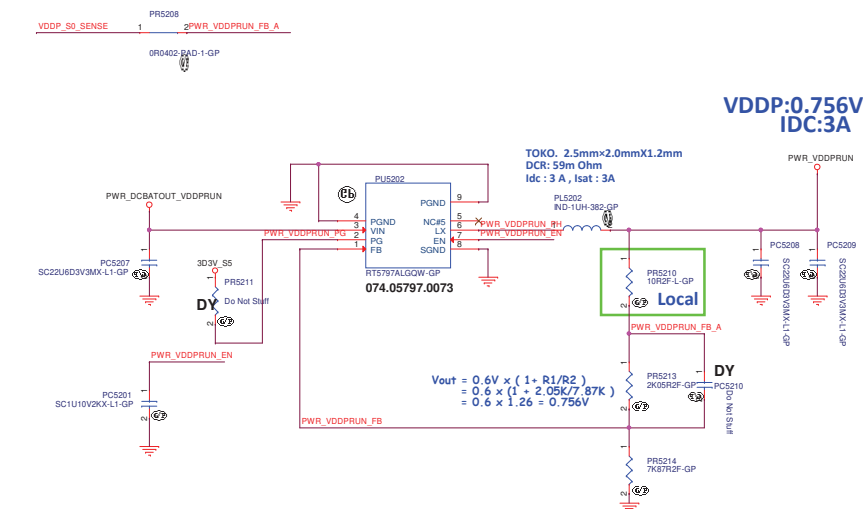
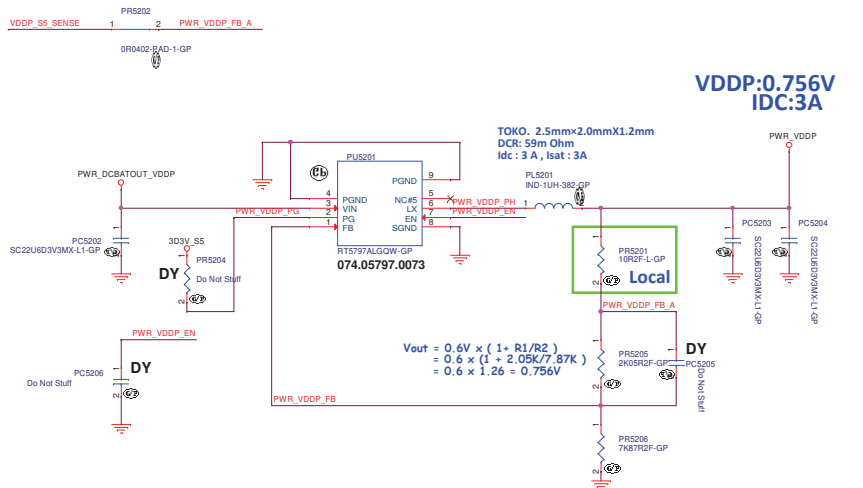
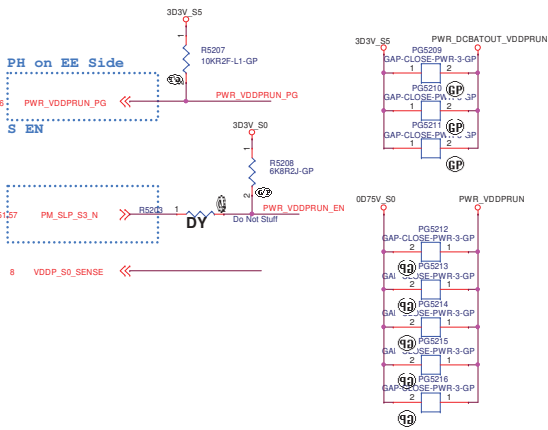
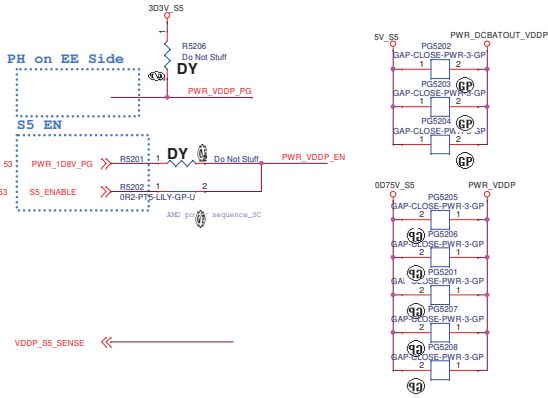


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

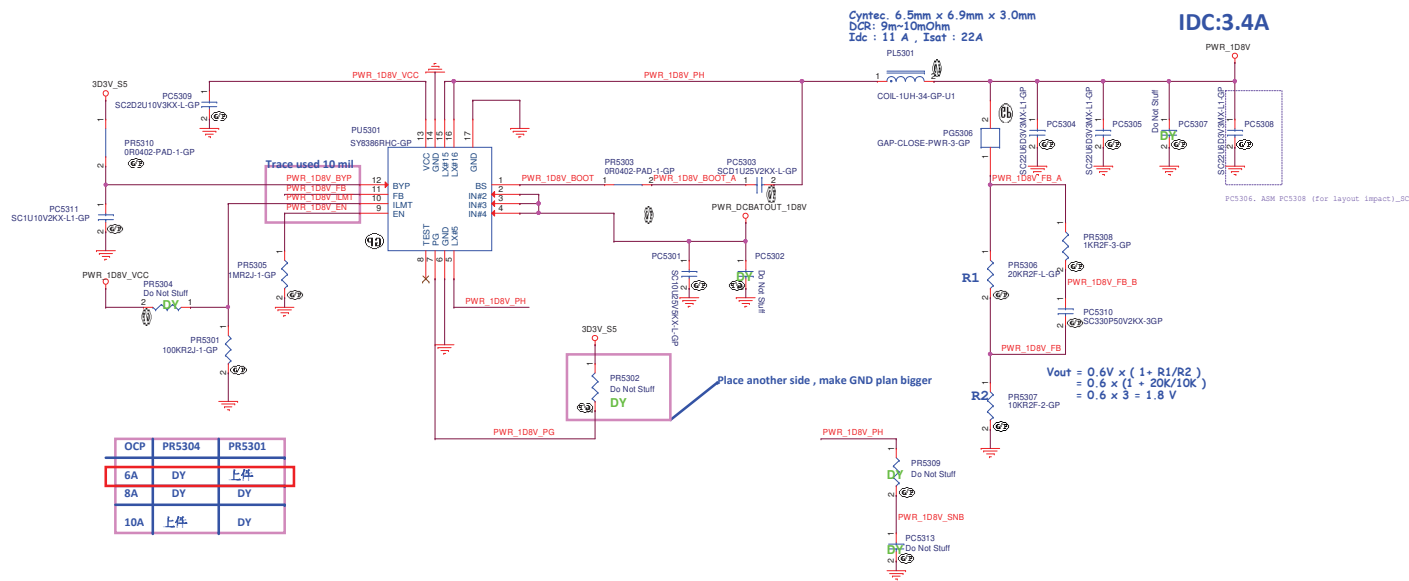
VID vs Vref Table
 VID Logic-High => Vref = 0.675 V
 VID Logic-Low => Vref = 0.75 V
 note: Vref can only be changed form 0.675v to 0.75v after power-on

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LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **POWER(RSVD)**

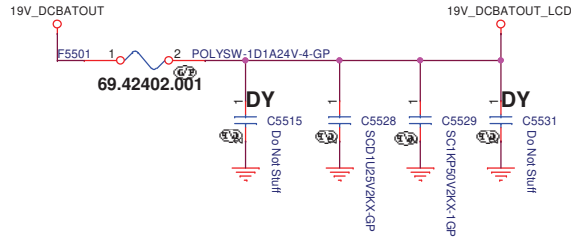
Size A4	Document Number LV550_AMD	Rev
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Date: Tuesday, April 20, 2021	Sheet 54 of 106
-------------------------------	-----------------

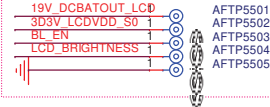
Main Func = LCD

INVERTER POWER

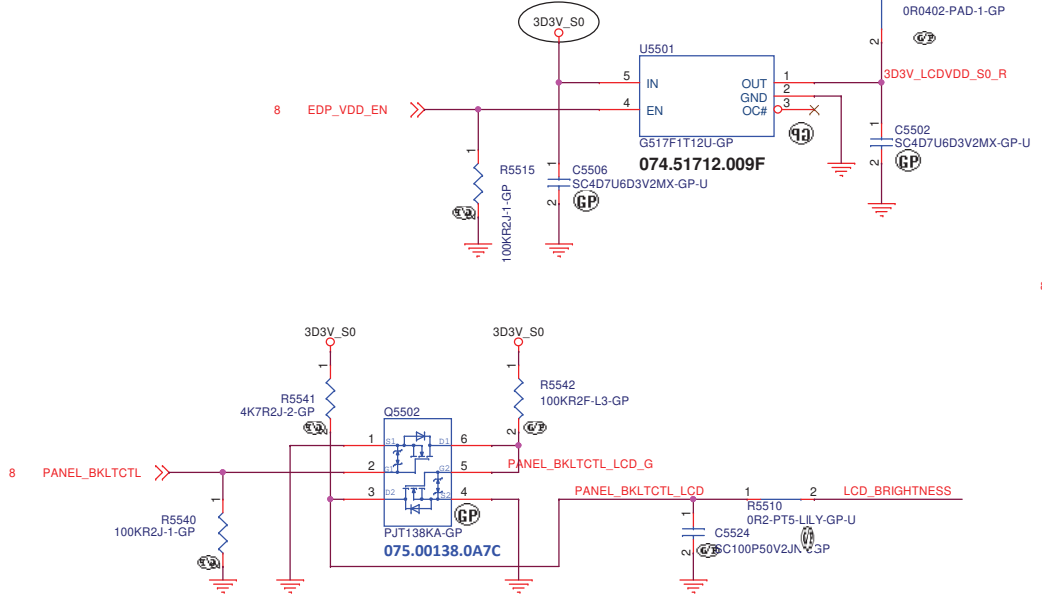
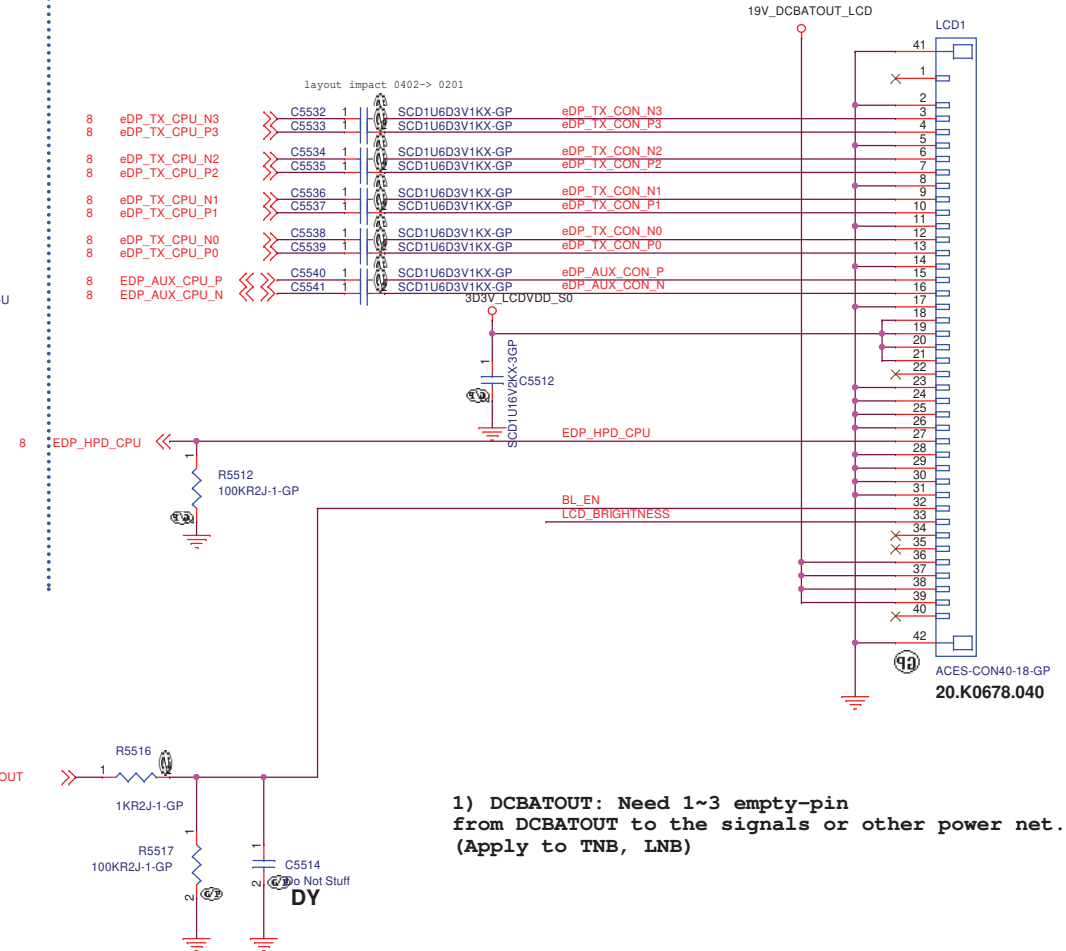
F5501 69.50007.A31->69.42402.001 (main)_20180718



Test point



LCD Connector

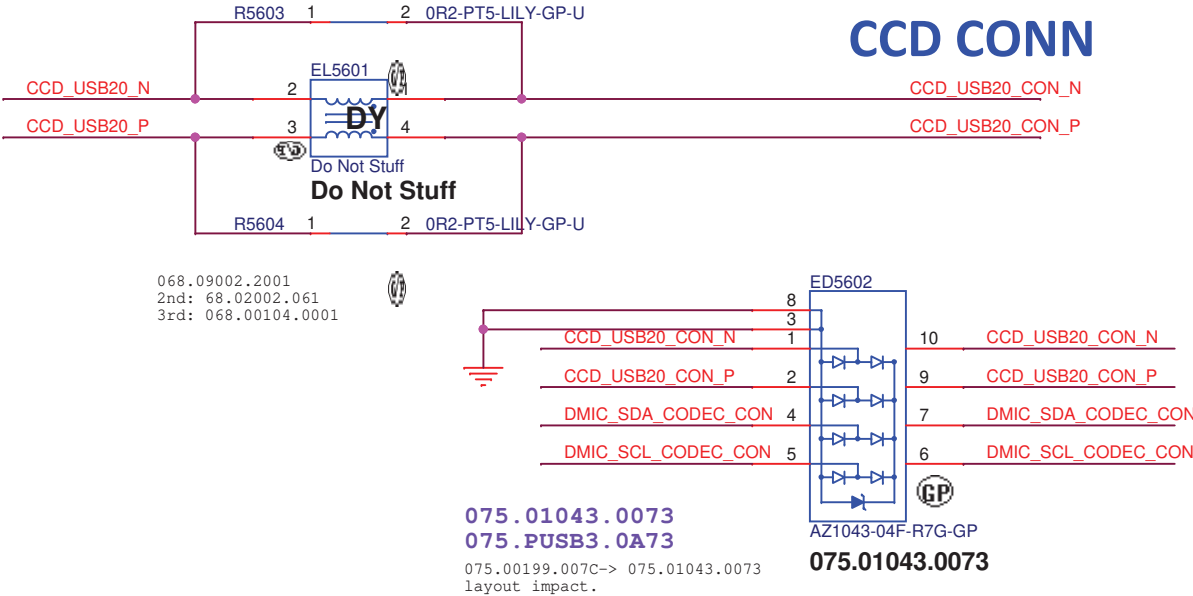


LV550AC

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title DISPLAY (LCD/TOUCH)		
Size A3	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021	Sheet 55 of 106	

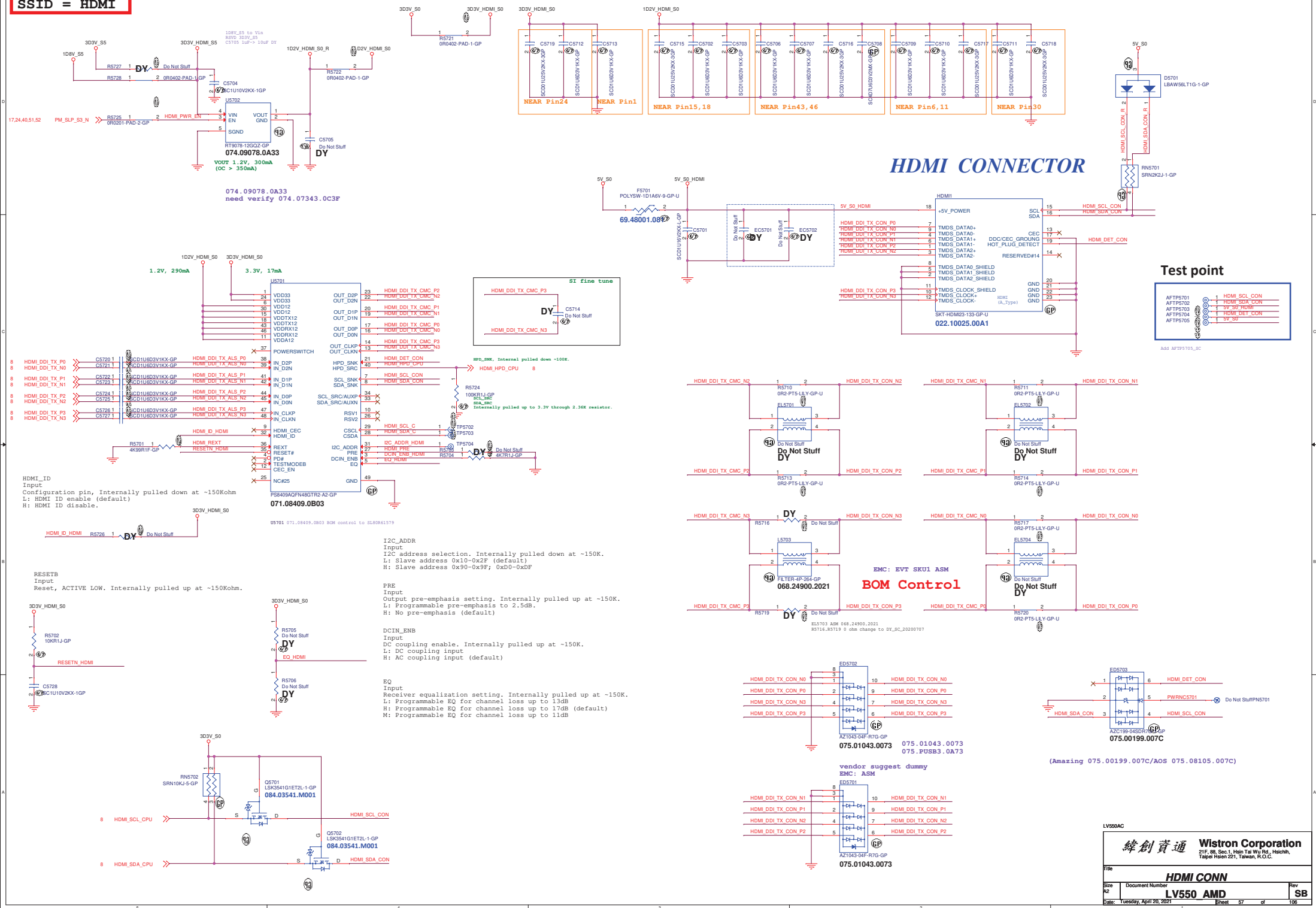
18	CCD_USB20_P	⋈	⋈	⋈	⋈
18	CCD_USB20_N	⋈	⋈	⋈	⋈
66	CCD_USB20_CON_N	⋈	⋈	⋈	⋈
66	CCD_USB20_CON_P	⋈	⋈	⋈	⋈
27,66	DMIC_SCL_CODEC_CON	⋈	⋈	⋈	⋈
27,66	DMIC_SDA_CODEC_CON	⋈	⋈	⋈	⋈



LV550AC

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Display (CRT/IR Camera)			
Size A4	Document Number LV550_AMD		Rev SB
Date:	Tuesday, April 20, 2021	Sheet 56 of	106

SSID = HDMI



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LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Display (RSVD)**

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 58 of 106

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Display (RSVD)		
Size	Document Number	Rev
A4	LV550_AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 59 of 106

(Blanking)

LV550AC

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (RSVD)

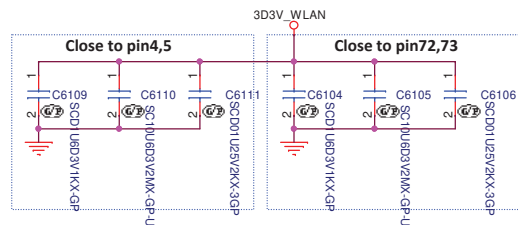
Size
A4

Document Number
LV550_AMD

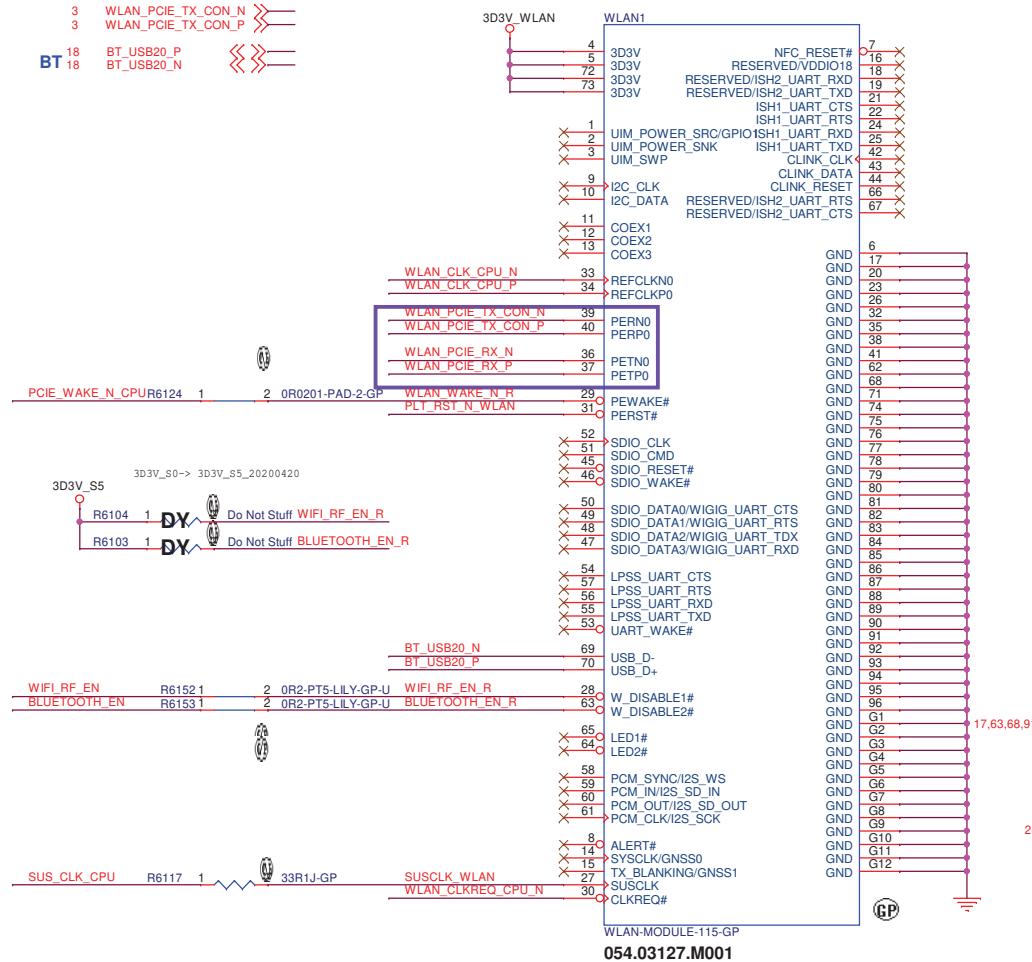
Rev
SB

Main Func = WLAN

- 16,24 WIFI_RF_EN
- 17,24 BLUETOOTH_EN
- 16 SUS_CLK_CPU
- 17 PCIE_WAKE_N_CPU
- 16 WLAN_CLKREQ_CPU_N
- 16 WLAN_CLK_CPU_N
- 16 WLAN_CLK_CPU_P
- 3 WLAN_PCIE_RX_N
- 3 WLAN_PCIE_RX_P
- 3 WLAN_PCIE_TX_CON_N
- 3 WLAN_PCIE_TX_CON_P
- 18 BT_USB20_P
- 18 BT_USB20_N

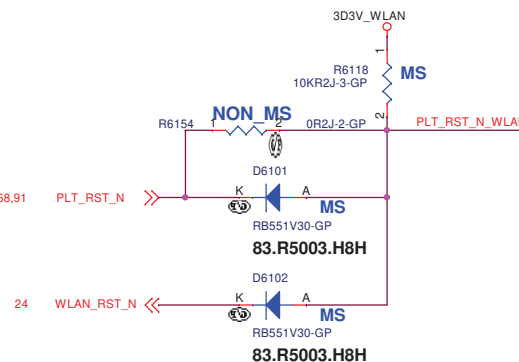
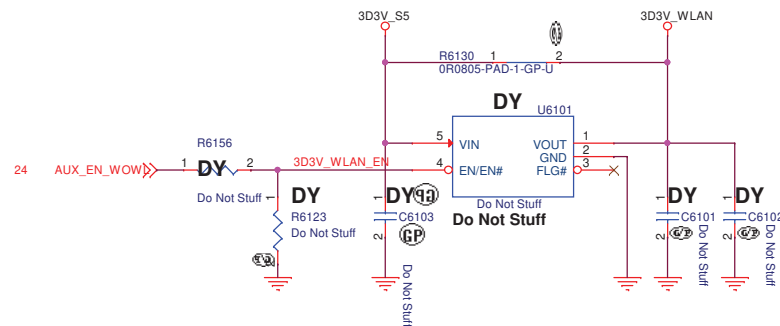


WLAN on board



BOM control to SW10MT3299 / SW10T06448

AOAC function circuit



Pin #	Pin Name platform pinout	Pin Name module pinout	Voltage on Card Side	WLAN, BT, or	Connection on Platform/Usage
30	CLKREQ#	CLKREQ#	3.3 V	WLAN	Also support 1.8 V electrical levels on this signal
31	PERST#	PERST#	3.3 V	WLAN	Also support 1.8 V electrical levels on this signal
32	GND	GND			
33	REFCLKN0	REFCLKN0	PCIE phy	WLAN	PCIE phy signals, use phy levels and not digital pins
34	REFCLKP0	REFCLKP0	PCIE phy	WLAN	PCIE phy signals, use phy levels and not digital pins
35	GND	GND			
36	PERN0	PETn0	PCIE phy	WLAN	PCIE phy signals, use phy levels and not digital pins
37	PERP0	PETp0	PCIE phy	WLAN	PCIE phy signals, use phy levels and not digital pins
38	GND	GND			
39	PETn0	PERn0	PCIE phy	WLAN	PCIE phy signals, use phy levels and not digital pins
40	PETp0	PERp0	PCIE phy	WLAN	PCIE phy signals, use phy levels and not digital pins
41	GND	GND			
42	CLINK_CLK	CLINK_CLK	CLINK phy (1 V)	WLAN	CLINK phy
43	CLINK_DATA	CLINK_DATA	CLINK phy (1 V)	WLAN	CLINK phy
44	CLINK_RESET	CLINK_RESET	3.3 V	WLAN	CoP also supports 1.8 V electrical levels on this signal
45	SDIO_RESET# (0)	SDIO_RESET# (I)	NA		Signal not used, leave NC in platform side
46	SDIO_WAKE# (I)	SDIO_WAKE# (0)	NA		Signal not used, leave NC in platform side
47	SDIO_DATA3 (IO)/WIGIG U ART_TXD (0)	SDIO_DATA3 (IO)/WIGIG U ART_RXD (I)	NA		Signal not used, leave NC in platform side
48	SDIO_DATA2 (IO)/WIGIG UART_RXD (I)	SDIO_DATA2 (IO)/WIGIG UART_TXD (0)	NA		Signal not used, leave NC in platform side

LV550AC

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

INT IO (WLAN M.2)		
Size A3	Document Number	Rev SB
LV550 AMD		
Date: Tuesday, April 20, 2021	Sheet 61	of 106

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title INT IO (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 62 of 106

Main M.2 SSD

3 SSD_PCIE_RX_N1 << >>
3 SSD_PCIE_RX_P1 << >>
3 SSD_PCIE_TX_CON_N1 << >>
3 SSD_PCIE_TX_CON_P1 << >>
3 SSD_PCIE_RX_N2 << >>
3 SSD_PCIE_RX_P2 << >>
3 SSD_PCIE_TX_CON_N2 << >>
3 SSD_PCIE_TX_CON_P2 << >>
3 SSD_PCIE_RX_N3 << >>
3 SSD_PCIE_RX_P3 << >>
3 SSD_PCIE_TX_CON_N3 << >>
3 SSD_PCIE_TX_CON_P3 << >>
3 SSD_PCIE_RX_N0 << >>
3 SSD_PCIE_RX_P0 << >>
3 SSD_PCIE_TX_CON_N0 << >>
3 SSD_PCIE_TX_CON_P0 << >>
16 SSD_CLK_CPU_N << >>
16 SSD_CLK_CPU_P << >>
16 SSD_CLKREQ_CPU_N << >>

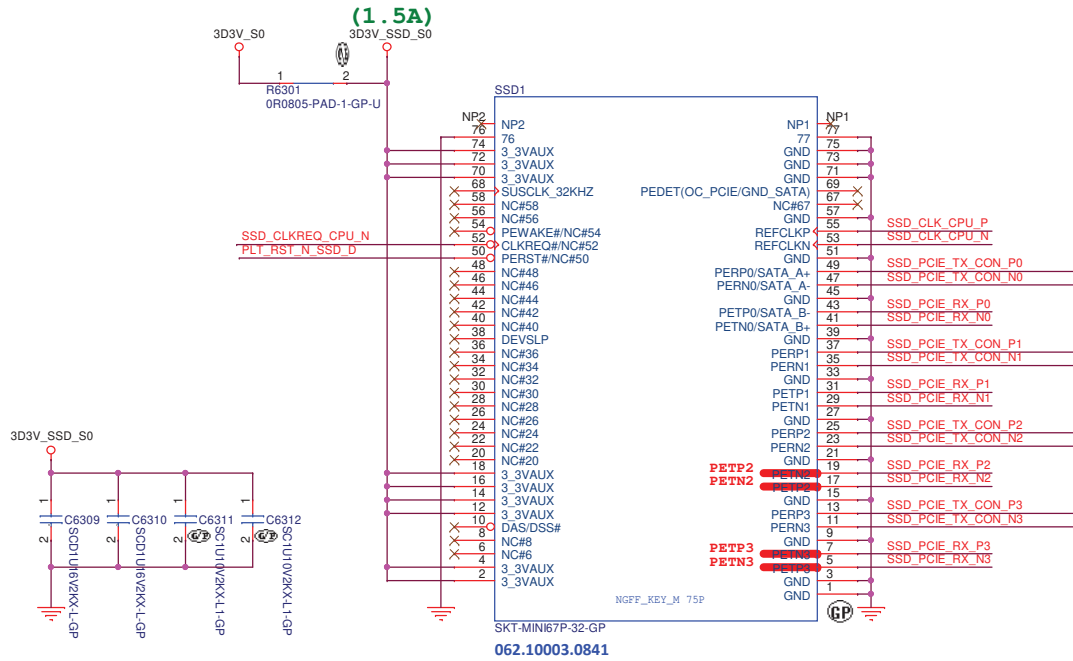
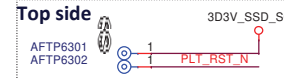
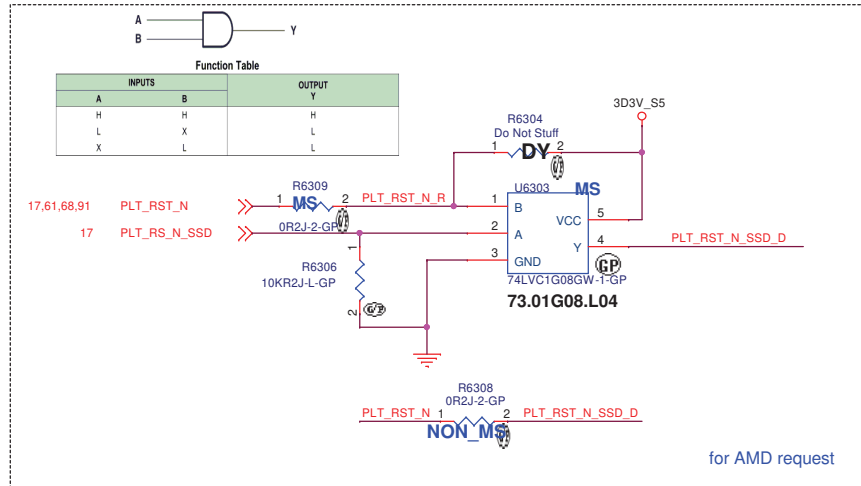


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32KHz) (O)(0/3.3V)	PEDET (NC_PCIE/GND_SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKp	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKn	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1



LV550AC

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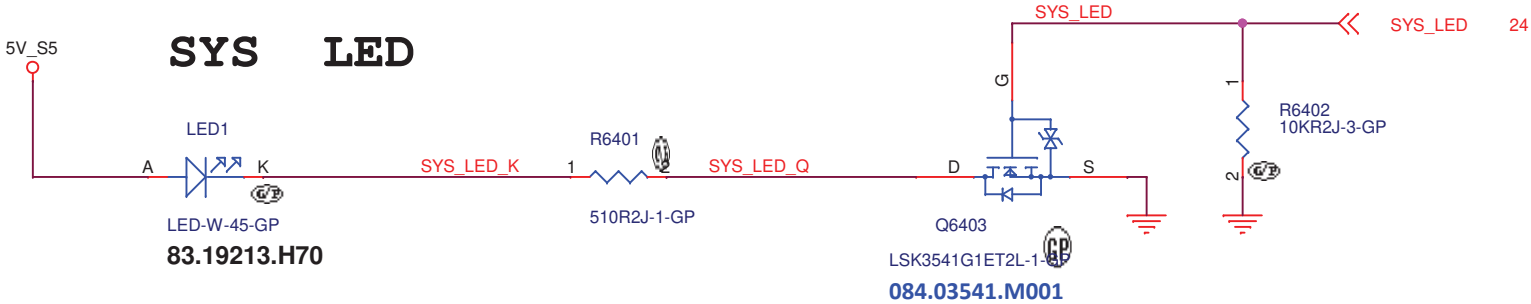
Title			INT IO (SSD M.2/ eMMC)
Size	Document Number	Rev	
A3	LV550 AMD	SB	
Date:	Tuesday, April 20, 2021	Sheet	63 of 106

LED

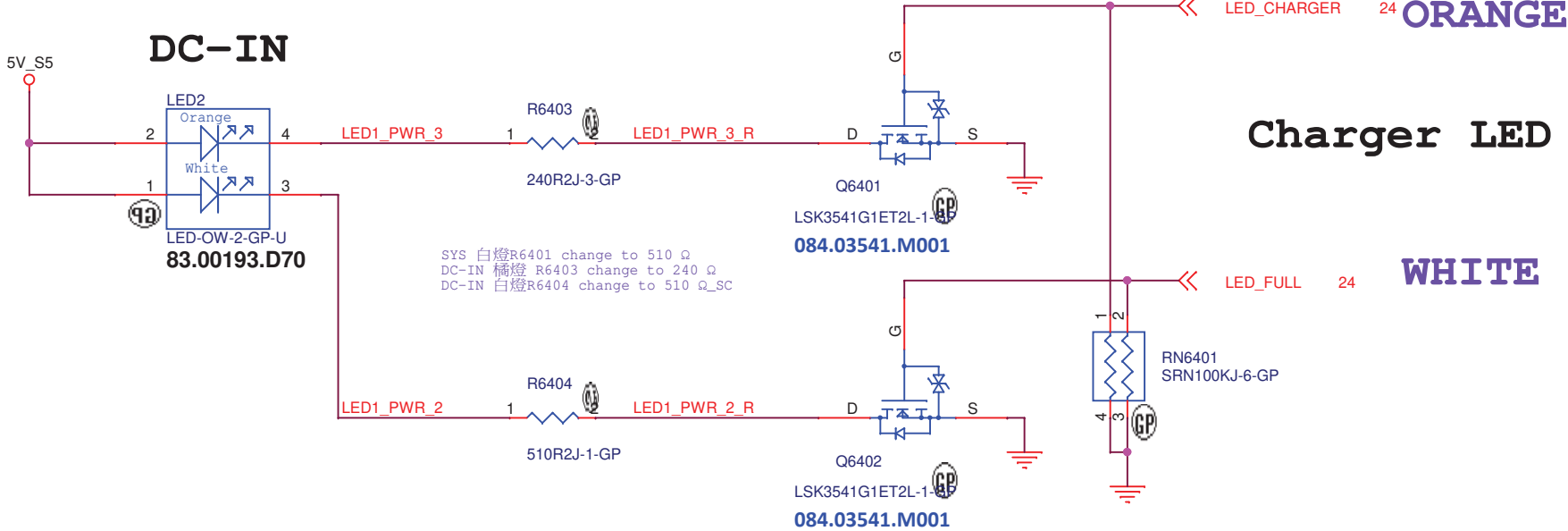
LED resistor

		13'	14'
DC-IN	ORANGE	150 OHM	250 OHM
	WHITE	300 OHM	250 OHM
SYS	WHITE	1.5K OHM	800 OHM
PWR BTN	WHITE	1K OHM	500 OHM
FP LED	GREEN	500 OHM	250 OHM

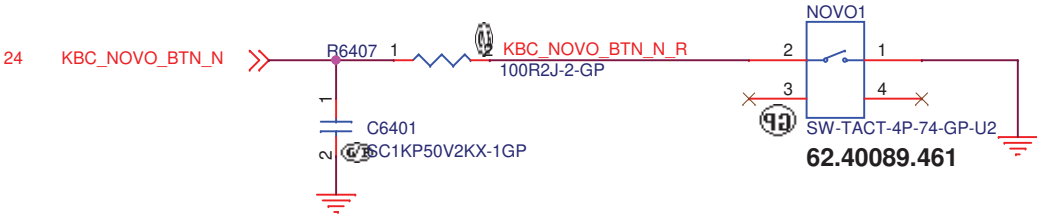
SYS LED



DC-IN



NOVO BUTTON



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Title

LED / Button / Power Button

SizeA4

Document Number

LV550_AMD

RevSB

Date: Tuesday, April 20, 2021

Sheet 64 of 106

24 KCOL[15:0] >>>

24 KROW[7:0] <<<



Title			
INT IO (KB/TP)			
Size A3	Document Number		Rev
	LV550 AMD		SB
Date:	Tuesday, April 20, 2021	Sheet 65 of	106

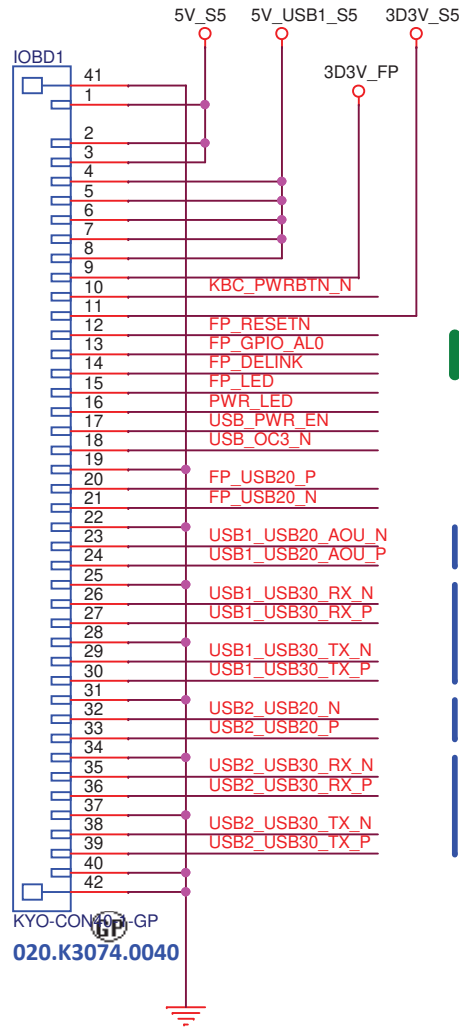
TYPEA Port1 AOU

18	USB1_USB30_TX_N	<<---
18	USB1_USB30_TX_P	<<---
18	USB1_USB30_RX_N	>>---
18	USB1_USB30_RX_P	>>---
36	USB1_USB20_AOU_P	<< >>---
36	USB1_USB20_AOU_N	<< >>---

TYPEA Port2

18	USB2_USB30_TX_N	<<---
18	USB2_USB30_TX_P	<<---
18	USB2_USB30_RX_N	>>---
18	USB2_USB30_RX_P	>>---
18	USB2_USB20_P	<< >>---
18	USB2_USB20_N	<< >>---

24	USB_PWR_EN	>>---
18	USB_OC3_N	<<---
24	KBC_PWRBTN_N	<<---
24	PWR_LED	>>---
24	FP_LED	>>---
18	FP_USB20_P	<< >>---
18	FP_USB20_N	<< >>---
24	FP_RESETN	<<---
24	FP_GPIO_AL0	<<---
24	FP_DELINK	<<---

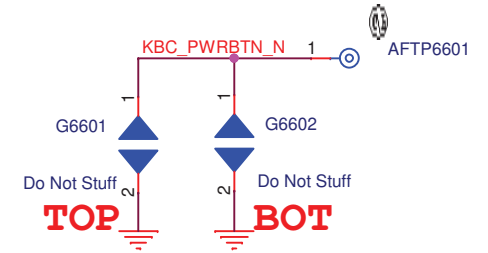
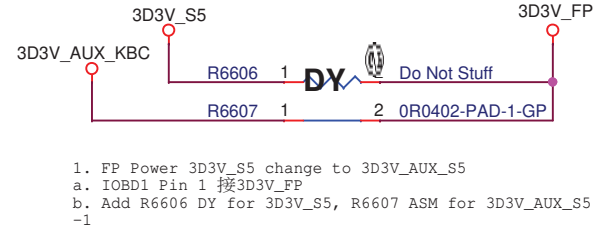


To EC.

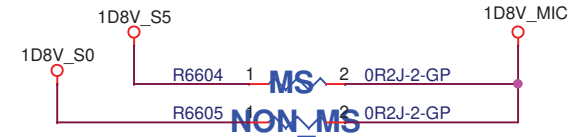
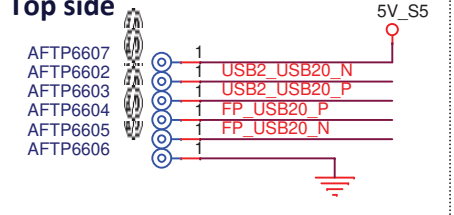
TYPEA Port1 AOU

USB2 USB20

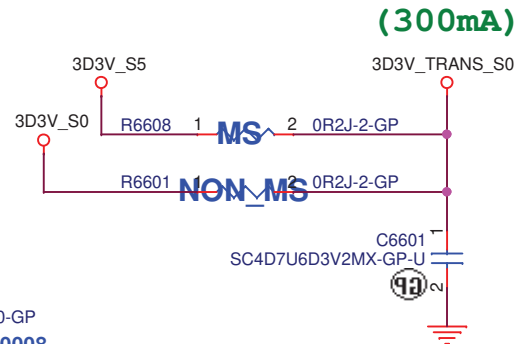
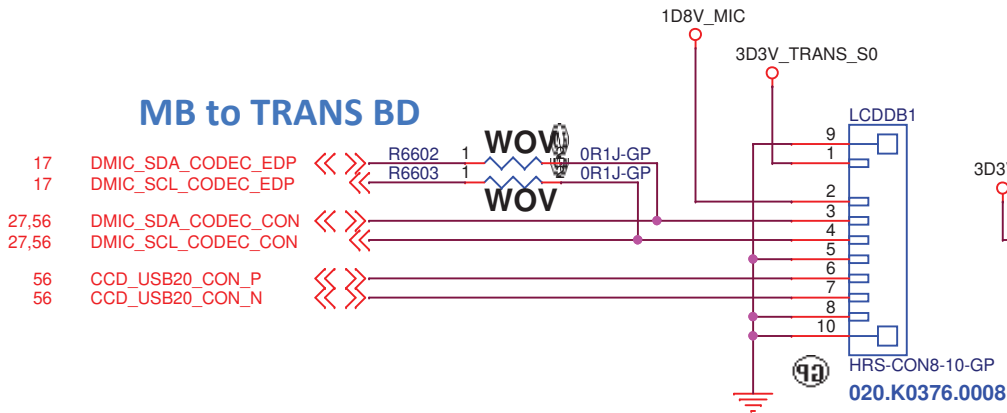
TYPEA Port2



Top side

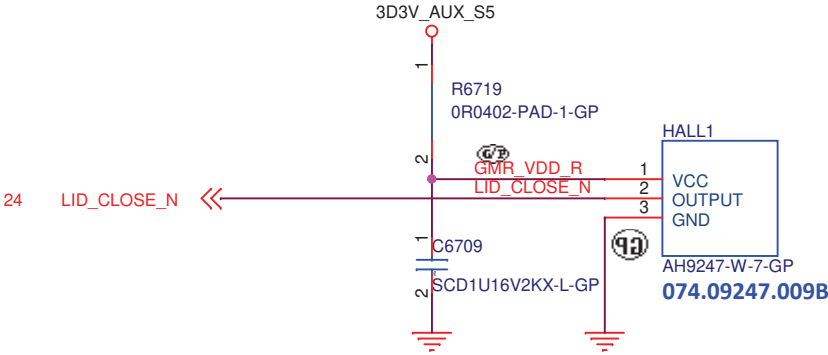


MB to TRANS BD



LV550AC

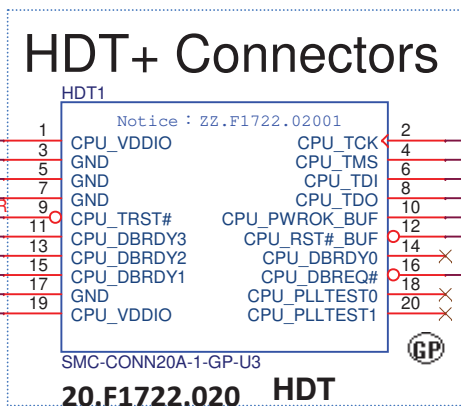
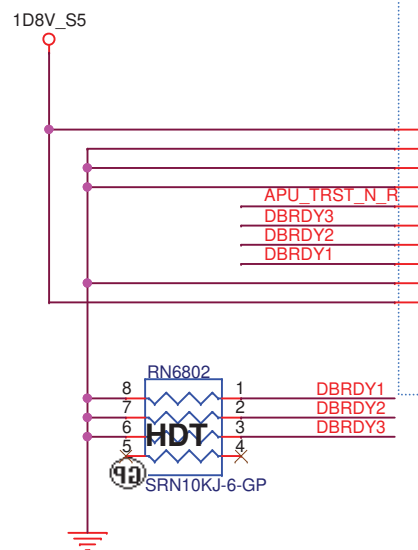
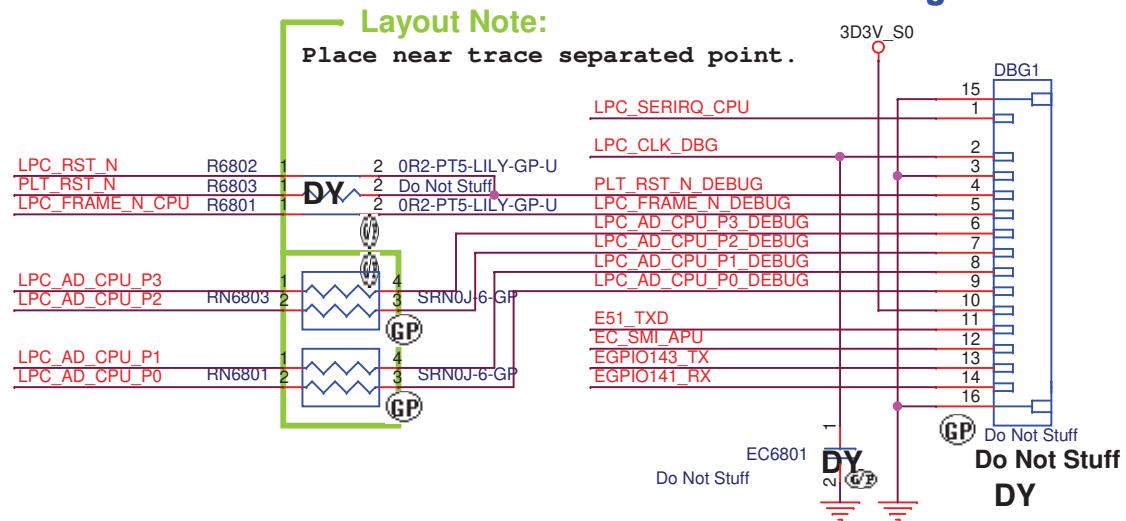
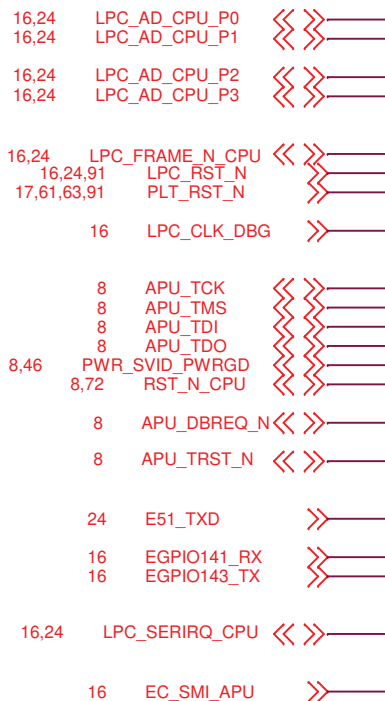
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IO BOARD CONN			
Size A4	Document Number LV550_AMD		Rev SB
Date: Tuesday, April 20, 2021		Sheet 66	of 106



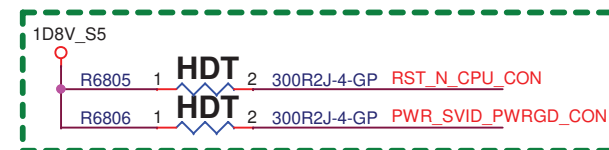
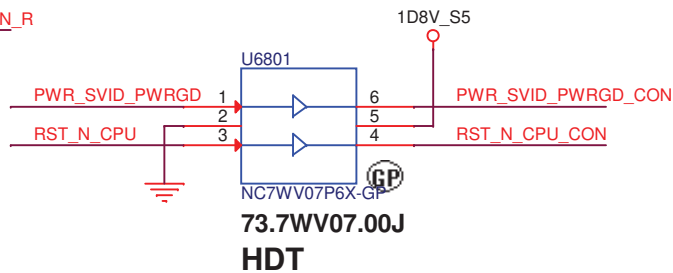
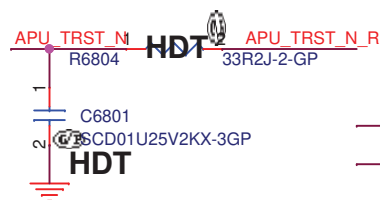
LV550AC

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Title <div>SENSOR (HALL-SENSOR)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		
Sheet 67 of 106		

SSID = DEBUG PORT



20.F1722.020: Dummy Pad with solder mask is ZZ.F1722.02001



LV550AC

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Title

Debug (LPC/HDT)

Size
A4

Document Number

LV550 AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 68 of 106

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LV550AC

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Title **Sensor (RSVD)**

Size
A4

Document Number **LV550_AMD**

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 69 of 106

(Blanking)

LV550AC

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Title **Sensor (G-sensor)(RSVD)**

Size
A4

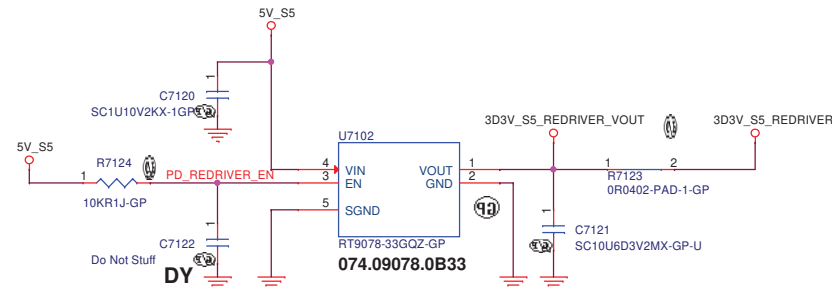
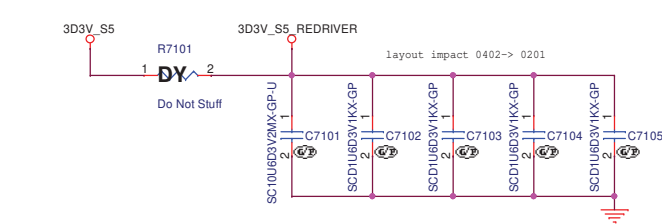
Document Number

LV550_AMD

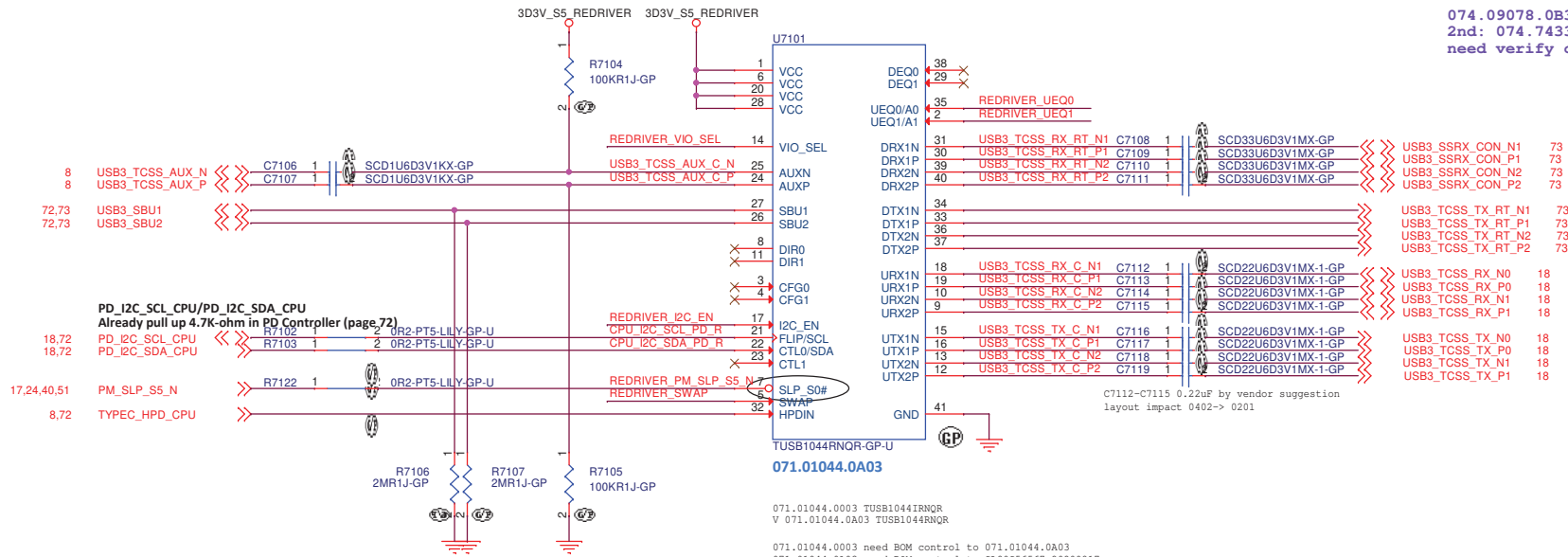
Rev
SB

Date: Tuesday, April 20, 2021

Sheet 70 of 106

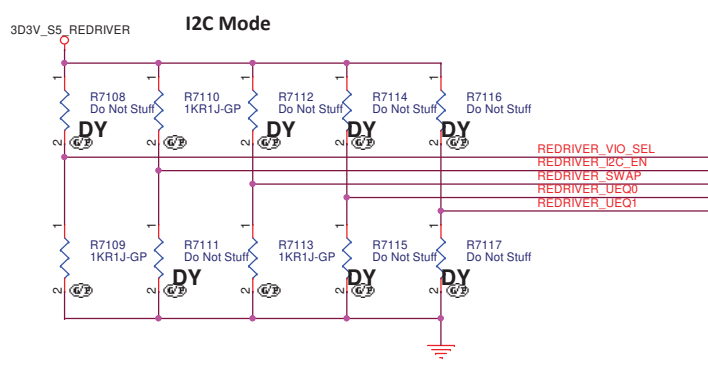


074.09078.0B33
2nd: 074.74333.0033
need verify common part: 074.07343.0F3F



To TYPEC USB3

HOST (From CPU)



I2C_EN: 1=I2C enabled
VIO_SEL: 0 = 3.3V configuration I/O voltage, 3.3V I 2C interface (Default)
SWAP: 0 - Do not swap channel directions and EQ settings (Default)
UEQ0/A0 and UEQ1/A1:FF

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Title

TYPE-C RE TIMER(1/2)

Size

A3

Document Number

LV550_AMD

Rev

SB

Date:

Tuesday, April 20, 2021

Sheet

71

of

106

(Blanking)

LV550AC

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Title		
EXT IO (TBT Re-Timer-2 RSVD)		
Size	Document Number	Rev
A4	LV550 AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 74 of 106

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Title EXT IO (TypeC Controller-2 RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 75 of 106

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Title GPU (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 76 of 106

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LV550AC

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Title
GPU (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 77 of 106

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Title <div>GPU (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 78 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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Title GPU (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 79 of 106

(Blanking)

LV550AC

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 80 of 106

(Blanking)

LV550AC

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Title GPU (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 81 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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LV550AC		
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Title GPU (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 82 of 106

(Blanking)

LV550AC

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **GPU (RSVD)**

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 83 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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LV550AC

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title GPU (RSVD)					
Size A4	Document Number LV550_AMD			Rev SB	
Date: Tuesday, April 20, 2021			Sheet 84	of	106

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LV550AC

緯創資通

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 85 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
GPU (RSVD)		
Size	Document Number	Rev
A4	LV550_AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 86 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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LV550AC		
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021		Sheet 87 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

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緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU (RSVD)					
Size	Document Number				Rev
A4	LV550_AMD				SB
Date: Tuesday, April 20, 2021			Sheet	88	of 106

H2
HOLE296R158-GP
ZZ.PAD01.V71



HS1
STF237R113H62-4-GP
34.4SE26.001



HOLE1
Do Not Stuff
Do Not Stuff



HOLE5
Do Not Stuff
Do Not Stuff



H5
HOLE296R158-GP
ZZ.PAD01.V71



HS2
STF237R113H62-4-GP
34.4SE26.001



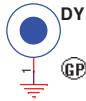
HOLE3
Do Not Stuff
Do Not Stuff



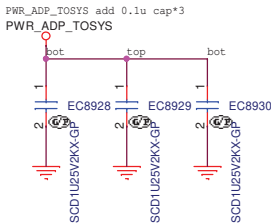
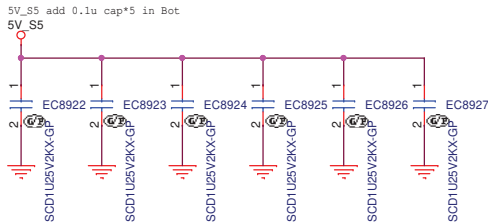
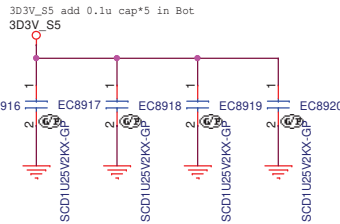
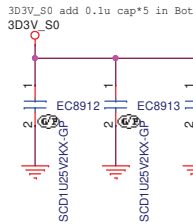
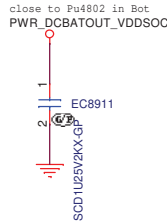
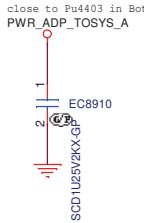
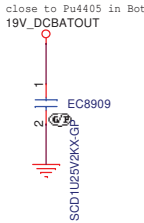
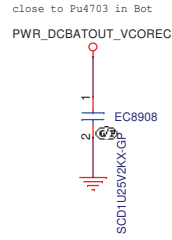
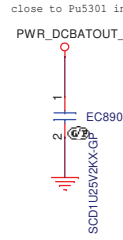
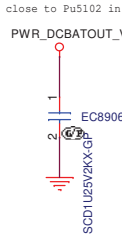
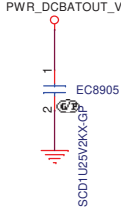
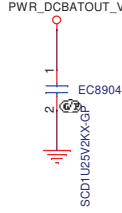
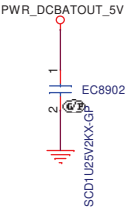
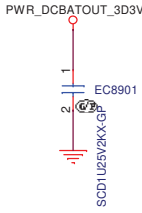
HOLE6
Do Not Stuff
Do Not Stuff



HOLE4
Do Not Stuff
Do Not Stuff



HOLE7
Do Not Stuff
Do Not Stuff



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Title UNUSED PARTS (RF/EMI Capacitors)			
Size A3	Document Number LV550 AMD		Rev SB
Date: Tuesday, April 20, 2021	Sheet 89	of 106	

(Blanking)

LV550AC

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Title

INT IO (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 90 of 106

(Blanking)

LV550AC

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Title INT IO (FP) (RSVD)		
Size A4	Document Number LV550_AMD	Rev SB
Date: Tuesday, April 20, 2021	Sheet 92 of	106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

(Blanking)

LV550AC		
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
EXT IO (RSVD)		
Size	Document Number	Rev
A4	LV550 AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 93 of 106

(Blanking)

LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EXT IO (RSVD)

Size
A4

Document Number

LV550 AMD

Rev

SB

Date: Tuesday, April 20, 2021

Sheet 94 of 106

(Blanking)

LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EXT IO (RSVD)

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 95 of 106

(Blanking)

LV550AC

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Commercial (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 96 of 106

(Blanking)

LV550AC

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Commercial (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 97 of 106

(Blanking)

LV550AC

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Commercial (RSVD)			
Size A4	Document Number LV550 AMD		Rev SB
Date: Tuesday, April 20, 2021		Sheet 98 of	106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service Review

(Blanking)

LV550AC

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Debug (RSVD)</div>		
Size <div>A4</div>	Document Number <div>LV550_AMD</div>	Rev <div>SB</div>
Date: Tuesday, April 20, 2021		Sheet 99 of 106

(Blanking)

LV550AC

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size
A4

Document Number

LV550_AMD

Rev
SB

Date: Tuesday, April 20, 2021

Sheet 100 of 106

LENovo CONFIDENTIAL Wistron Taipei to Lenovo service review

(Blanking)

LV550AC

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Change History		
Size	Document Number	Rev
A4	LV550_AMD	SB
Date:	Tuesday, April 20, 2021	Sheet 101 of 106

(Blanking)

LV550AC

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Sequence

Size
A4

Document Number

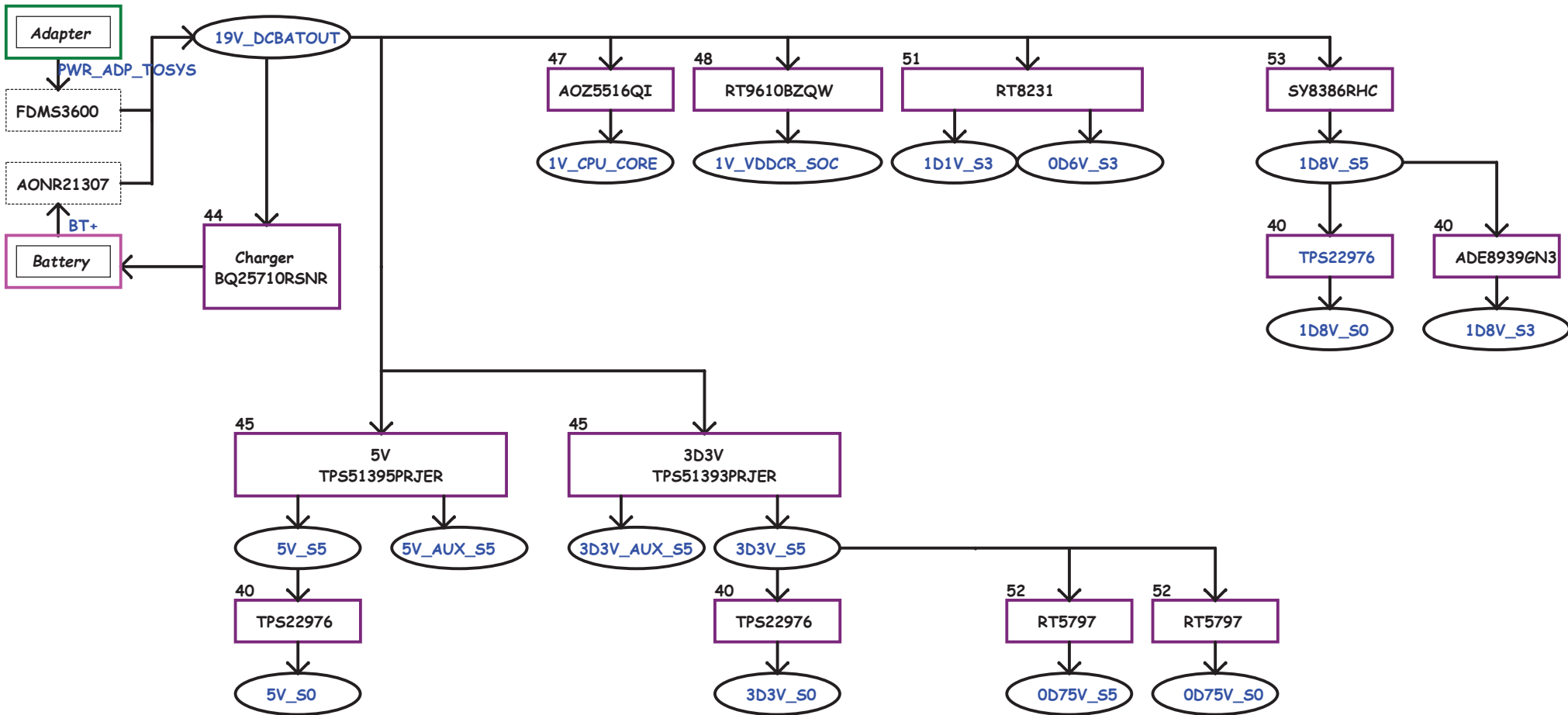
LV550_AMD

Rev

SB

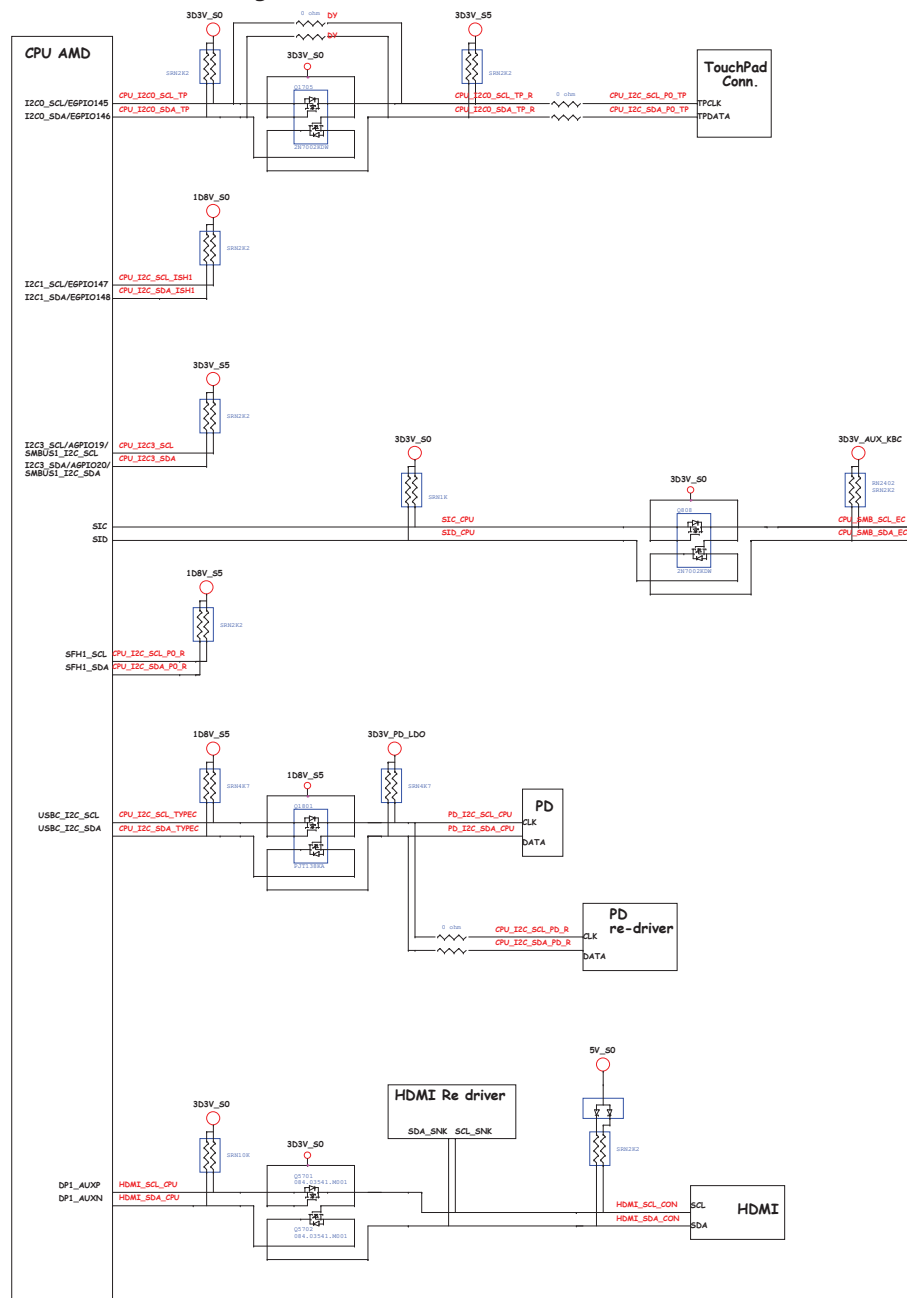
Date: Tuesday, April 20, 2021

Sheet 102 of 106

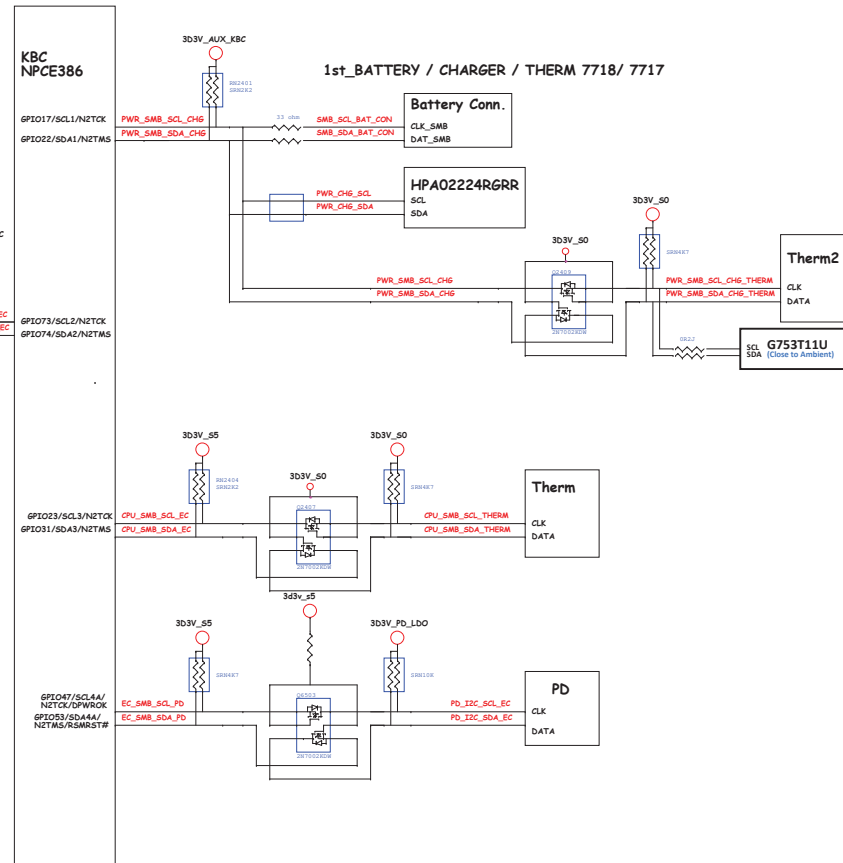


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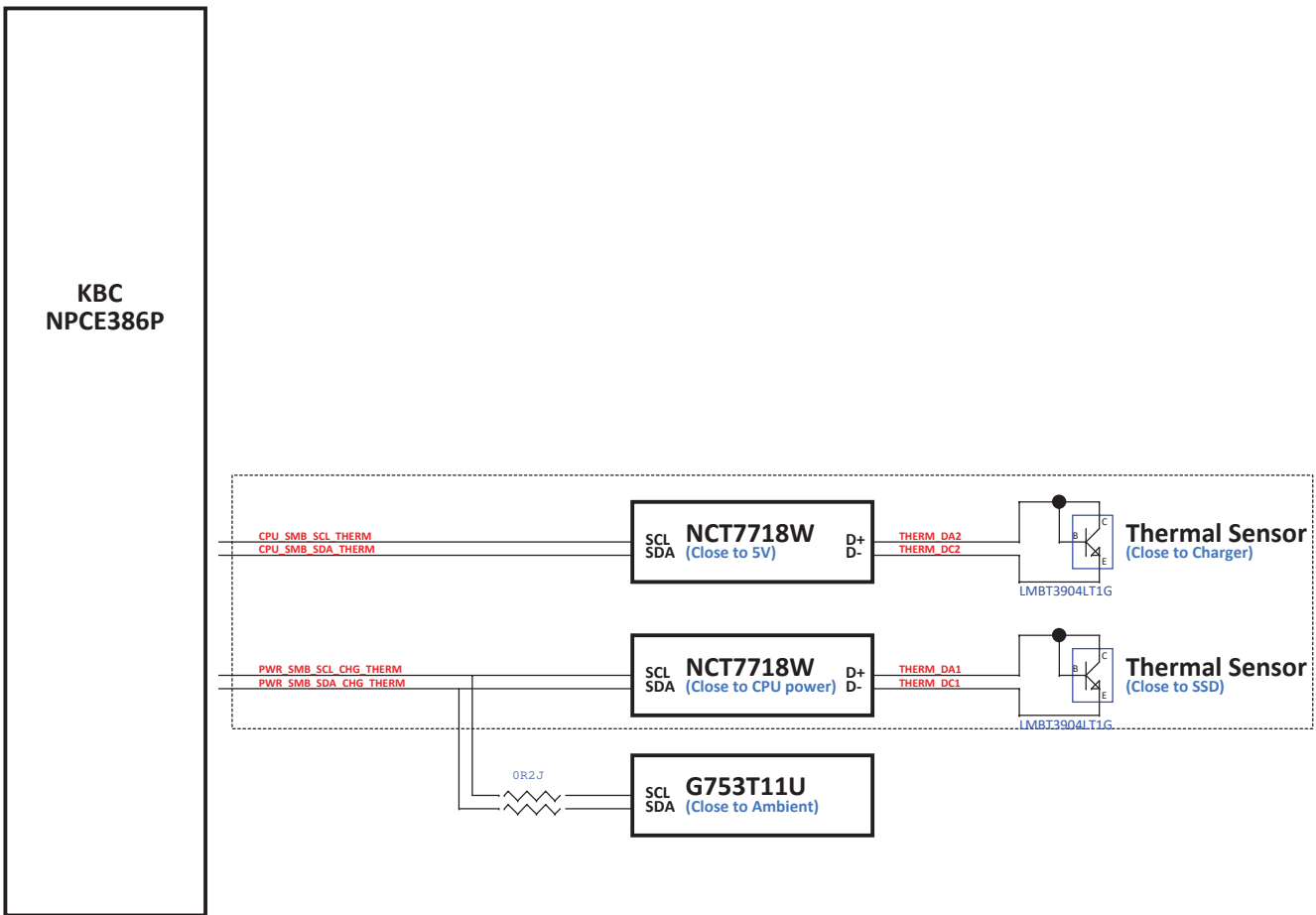
PCH SMBus Block Diagram



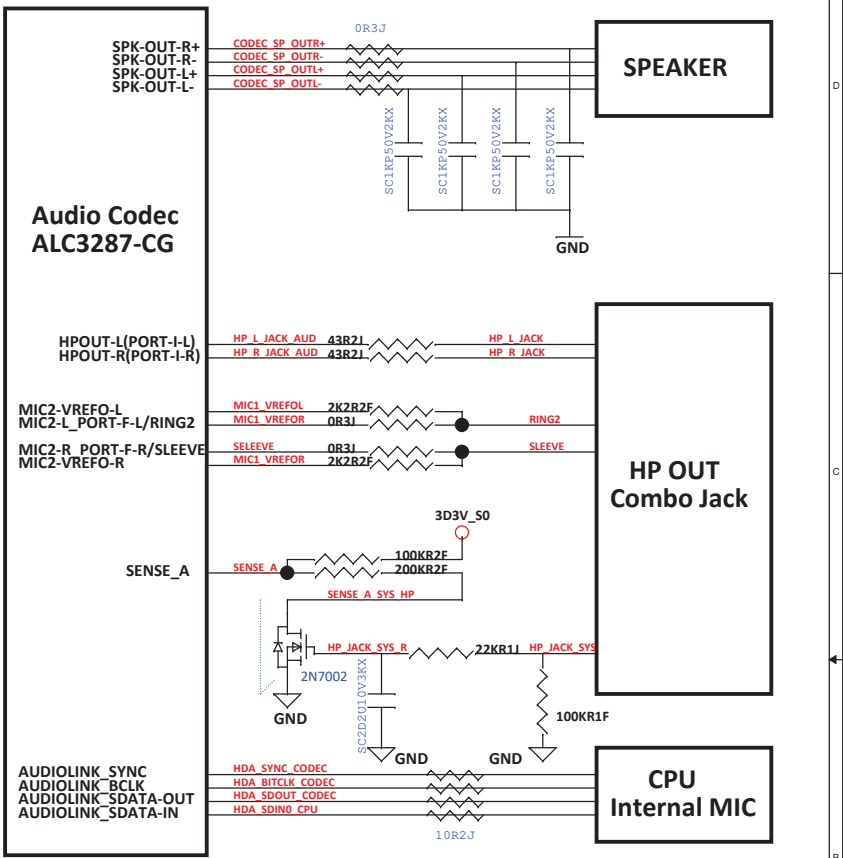
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



CLK Block Diagram

